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DIGITAL CIRCUITS

Lecture synopsis for studying the credit module of

«Digital circuits»

discipline

Recommended by the Methodical council of Igor Sikorsky KPI as a tutorial for students, who study in specialty 163 - Biomedical Engineering, specialization "*Clinical Engineering*"

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DIGITAL CIRCUITS

Lecture synopsis for studying the credit module of «Digital circuits» discipline

Compilers: ***Zubchuk: Viktor Ivanovich***, Ph.D., associate professor

Delavar-Kasmai Mohammad, Ph.D., senior lecturer

In the series of lectures the theoretical bases, principles of functioning and calculations of the main functional nodes of digital circuits technique methods are considered by sections: electronic switches on diodes and transistors, logical elements on the principles, DTL-, TTL-, ECL-, MOS- and I^2L- technology, code converters, including encoders, decoders, multiplexers, demultiplexers, combination adders, digital comparators, major trigger types (synchronous and asynchronous RS-, D-, JK-triggers), registers, asynchronous and synchronous counters, pulse devices for the detection, generation and generation of pulses, digital-to-analog and analog-to-digital converters.

Contents

1. Logic switches

Technical implementation of digital circuits, in which the signals are presented as discrete quantum levels of voltage (current), is based on the use of electronic voltage (current) commutators, are called logic switches.

As nonlinear devices with controlled resistance in logic switches, semiconductor diodes, transistors, phototransistors, thyristors, optrons, and electronic lamps are used.

1.1. Diode as a switch

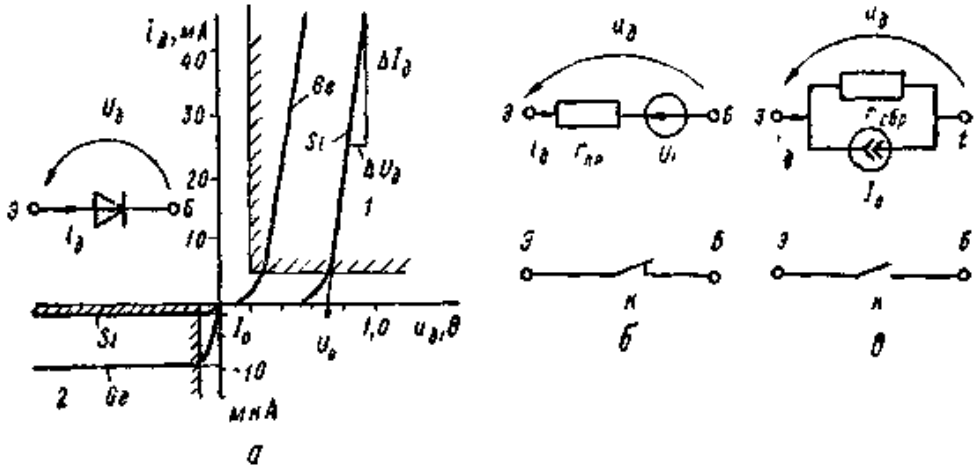


Fig. 1.1

In diode switches we use, dependence of diode resistance to magnitude and sign of the applied voltage. In fig. 1.1. (*а*) is shown typical static current–voltage characteristics (I–V curve) of germanium (Ge) and silicon (Si) diodes, and in Fig. 1.1. (*б*) and (*в*) are equivalent circuits for replacing a diode with a direct current for linearized (allocated by hatching) areas, respectively, 1 and 2. The current of the p-n-junction and the diode and the voltage $U_д$ on it are related by the ratio:

$$i_д = I_0\{exp\,[U_д / (m\,\varphi_T)] - 1\} = I_0\{exp\,[U_д\,q\,/(m\,k\,T)] - 1\}, \qquad (1.1)$$

where I_0 - thermal current saturation;

φ_T - Temperature potential (at normal temperature $T = 298\ ^\circ K$, $\varphi_T = 26\ mV$);

k - Boltzmann's constant;

T - Absolute temperature;

q - Charge of an electron.

m - is the coefficient taking into account the influence of surface currents of leakage of germanium diodes and generation and recombination currents in the p-n transition of silicon diodes (for germanium diodes $m_{Ge} \approx 1.2 \ldots 1.5$, for silicon - $m_{Si} \approx 1.2 \ldots 2$). The thermal current saturation I_0 practically does not depend on the voltage

applied to the diode and is determined by the electrophysical properties of the semiconductor material and its heating temperature:

$$I_0 = I_{00} \exp [- U_k / \varphi_T)],$$

where I_{00} is the constant due to the material of the semiconductor and the concentrations of impurities;

U_k - contact potential difference (U_k *(Ge) = 0.3 ... 0.4 V,* U_k *(Si) = 0.6 ... 0.7 V*).

The thermal current saturation I_0 exponentially increases with increasing temperature. In approximate calculations it is assumed that the current I_0 in the case of a germanium diode doubles with an increase in temperature for every 10 ° C, and in the case of silicon - every 7 ° C.

Taking into account the active resistance of the p- and n-regions, the contact resistances of the outputs and the ratio (1.1) for the real diode:

$$U_\partial = U_0 + i_\partial r = m \varphi_T \ln(i_\partial / I_0 + 1) + i_\partial r, \qquad (1.2)$$

where r is the total active resistance of the p – n- regions and contacts of the diode.

The differential active resistance of the diode will be obtained from the expression (1.2):

$$r_\partial = dU_\partial / di_\partial = m \varphi_T / (I_0 + i_\partial) + r,$$

The resistance r_∂ is nonlinear and depends on the current of the diode. But at sufficiently large direct-bias voltages ($U_\partial >> U_к$), the resistance $r_\partial \approx r$, i.e. the resistance of the equivalent diode replacement circuit (Fig. 1.1. (б)) $r_{пр} \approx r$ and has the order of units and tens of ohms. At the inverse displacement of the diode ($U_\partial < 0$) $i_\partial \approx 0$, $r_\partial = r_{обр} = m\varphi_T / I0 + r \approx m \varphi_T / I_0$ and is in the order of tens and hundreds of $k\Omega$.

The voltage U_0 of the equivalent voltage source in the substitution scheme (Fig. 1.1-б) is obtained by extrapolation of the quasilinear regions of the region 1 I–V curve to the intersection with the abscises axe, and it has the order of the contact potential difference: $U_0 \sim U_k$.

The scheme of the simplest diode switch, controlled by the source of the signal U_1 and loaded on the resistance $R_н$, is shown in Fig. 1.2-*а*, and in fig. 1.2-б, and *в*-equivalent circuit of the substitution respectively for the logic signal "1" and "0" at the input.

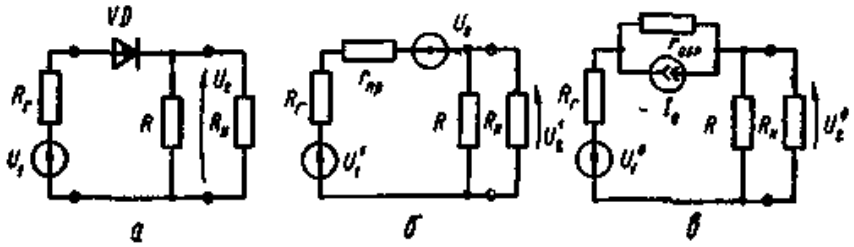


Fig. 1.2

Determine the value of the output voltages in each of the states of the switch, using the principle of superposition. At low input voltage, level ($U^0_1 << 0$) the diode *VD* is closed, the switch is open (Fig 1.2-*в*) and at its output set the low level:

$$U^0_2 = U^0_1[(R||R_н) / (R_г + r_{обр} + R||R_н)] - I_0[r_{обр}||(R||R_н + R_г)], \qquad (1.3)$$

Since usually $r_{обр} >> R$, $R_н$ can be approximated to be $U_2^0 \approx -I_0 (R \,||\, R_н)$.

At high level of input signal U_1^1 the diode VD is open, the switch is closed (Fig 1.2.-б) and the switch output has a high level:

$$U^1_2 = [(U^1_1 - U_0)(R||R_н)] / [R_г + r_{пр} + R||R_н], \qquad (1.4)$$

Since usually $r_{пр} << R$, $R_н$ can be considered approximately $U_2^1 \approx U_1^1 - U_0$.

From the relations (1.3) and (1.4) it is seen that the voltage drop across the output: $\Delta U_2 = U^1_2 - U^0_2 < \Delta U_1 = U^1_1 - U^0_1$ (less than U_0). The attenuation of the output signal is greater, the greater the resistance of the signal source $R_г$. The disadvantage of the diode switch in Fig. 1.2 is the direct dependence of the level U^1_2 on the input signal U^1_1.

The second variant of the diode switch is shown in Fig. 1.3. At the low level of the input signal, the diode *VD* is open and the current of the power source U_{un} flows through it, which is limited to the resistance *R*. If $R >> R_г$, then virtually the entire supply voltage U_{un} falls on the support *R*, so the low potential U^0_2 (Fig. 1.3-б) is set on the load support of the $R_н$ switch:

$$U^0_2 = U_{un.}[(R_н||(R_г + r_{пр})) / (R + R_н||(R_г + r_{пр}))] + (U^0_1 + U_0)[(R||R_н) / (R_г + r_{пр} + R||R_н)].$$

If $R_г + r_{пр} << R||R_н$, then $U^0_2 \sim U^0_1 + U_0$.

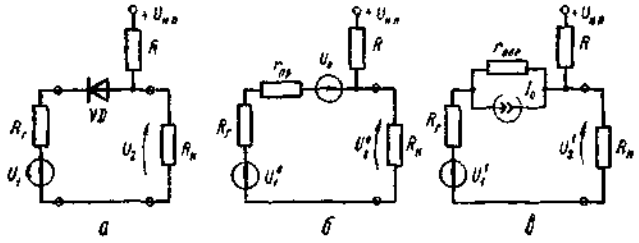


Fig. 1.3

At a high level of the input signal, if the condition $U^1_1 > U_{un} R_н / (R + R_н)$, the *VD* diode is closed, the input circuit is disconnected from the load (Fig. 1.3-*в*) and the output voltage is set to high:

$U^1_2 = U_{un}[(R_н||(r_{обр} + R_г)) / (R + R_н||(r_{обр} + R_г))] + U^1_1[R||R_н / (R_г + r_{пр} + R||R_в)] + I_0(R||R_н||(R_г + r_{обр}))$,

Usually $r_{обр} >> R_г$, $R_н$, so $U^1_2 \approx (U_{un} + RI_0) R_н / (R + R_н)$ and it does not depend on the input signal. Note that if in the circuit diagram of Fig. 1.2 the low output signal is $U^0_2 \approx 0$, and the high depends on the input signal U^1_1, then in the circuit diagram of Fig. 1.3, on the contrary, the low level $U^0_2 \approx U^0_1 + U_0$ is proportional to the input signal, and the high U^1_2 does not depend on it.

Considered diode switches can be used to construct the simplest combinational logic circuits. In Fig. 1.4-a shows the scheme, and in Fig. 1.4-б the truth table and conditional graphic designation of a two-input logic element OR on diode switches. Only in the case when on both inputs have low level U^0_{11} and U^0_{12}, diodes *VD1*, *VD2* are closed, the output is disconnected from the inputs, and is set to low. In any other combination, the output connects to the input to which the highest level is given, i.e. $U_{12} \approx max\{U_{11}, U_{12}\} - U_0$. This expression is an analogue expression of disjunction.

Scheme on Fig 1.4-*в* - variant of the switch on Fig. 1.3 for two inputs. If at least one of the *VD1* diodes, *VD2* is open by a low input signal, the circuit output is connected to the lowest input. Only when all the diodes are locked up by high levels at the inputs, the output circuit is disconnected from the inputs and the load is set to high potential. As can be seen from the truth table on Fig. 1.4-*г*, such a scheme implements a logical operation of conjunction. Its analog equivalent is determined by the expression $U_{02} \approx min\{U_{11}, U_{12}\} + U_0$

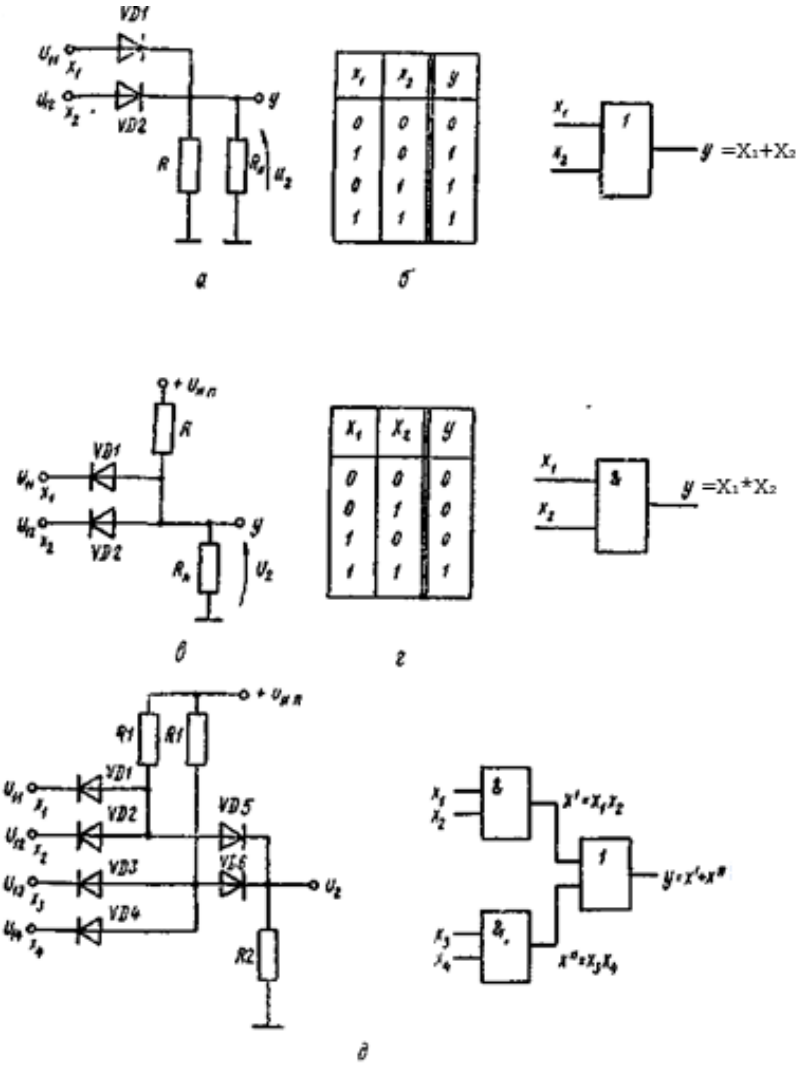


Fig. 1.4

Based on diode switches, two-step combinational logic elements are constructed. Listed in Fig. 1.4-*д* scheme implements the logical function $y = x_1x_2 + x_3x_4$ or for electric signals $U_2 \approx max\{min[U_{11}, U_{12}], min[U_{13}, U_{14}]\}$. Since the circuit consists of passive components, the input signal is weakened by passing each logical degree. In order for the amplitude of the output signal U_2 to be maximal, it is necessary to fulfill the conditions $R_1 << R_2 << R_н$, which inevitably leads to an increase in the power consumption of the circuit.

1.2. Bipolar transistor as a switch

The use of bipolar transistors in electronic switches is based on the properties of transistors to change the resistance of a very large (hundreds of kΩ) in a Cut-off mode to significantly less, in an active mode (kΩ units) and very small in saturation mode (units of Ω) under the action of the control signal.

In Fig. 1.5-*а* shows the static characteristics of the bipolar transistor when included in the scheme with a common emitter (CE); on Fig 1.5-б - input characteristics $I_Б = f_1(U_{бе})$ while $U_{кe}$ = const; in Fig 1.5-*в* - output characteristics $i_к = f_2(U_{кe})$ while $I_б = const$. The transistor in switch devices operates in a high signal mode and its properties can be described by a nonlinear Ebers-Molla injection model of ideal diodes and controlled current sources (Fig. 1.6).

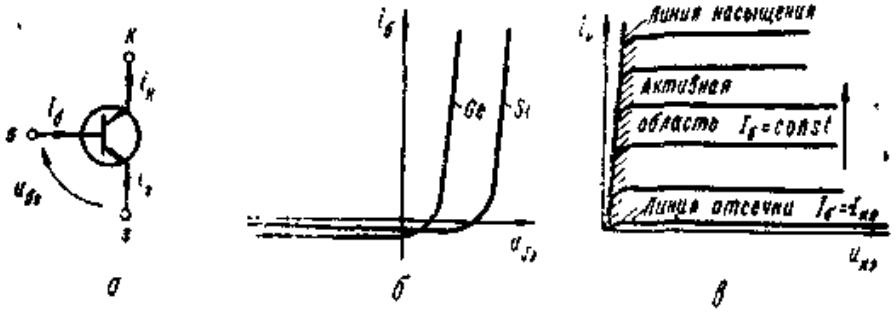


Fig. 1.5

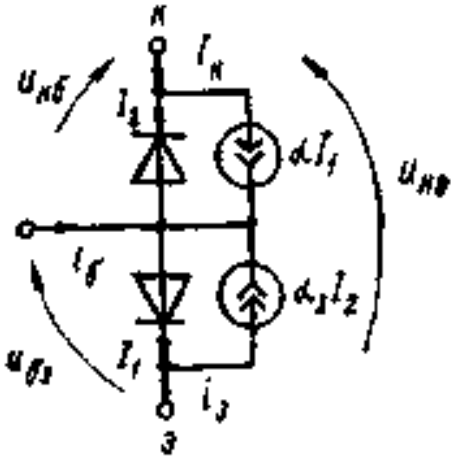


Fig.1.6

The current of electrodes of the transistor, depending on the voltage on them, are determined by the relations:

$$\begin{cases} i_c = [(I_{k0}\alpha_I) / (\alpha\,(1 - \alpha\alpha_I))]\;[(\exp(\lambda U_{be}) - 1) - \alpha\,(\exp(\lambda U_{cb}) - 1)]; \\ i_э = [I_{k0} / (1 - \alpha\alpha_I)]\;[(\exp(\lambda U_{be}) - 1)\,\alpha_1 - \exp(\lambda U_{cb}) + 1)]; \\ i_b = i_e - i_c, \end{cases}$$

where: $\lambda = 1 / (m\varphi_t)$;

$I_{к0}$ - collector reverse current;

α and α_I - emitter current transfer coefficients in the collector circuit, respectively, in normal and inverted active modes.

Such model is used mainly in machine design methods, and in approach calculations, piecewise linearly approximated models are used.

Let's consider the scheme of the simplest switch on the bipolar transistor of npn-type (Fig. 1.7-*a*). The load on the transistor *VT* is a resistor connected between the output and the common bus ($R''_н$), or between the output and the power supply ($R'_н$), or the load can be divided ($R'_н$, $R''_н$). The mode of operation of the transistor is determined by the sources of the input signal $U_г$ and the input circuit of the resistors *R1*, *R2* and the source of the closing offset - U_{un2}. The *R1* and *R2* resistors must be selected so that, at low input levels, the U^0_1 transistor *VT* is reliably locked throughout the operating range of ambient temperatures, and at high U^1_1 level, the transistor must be saturated at the input.

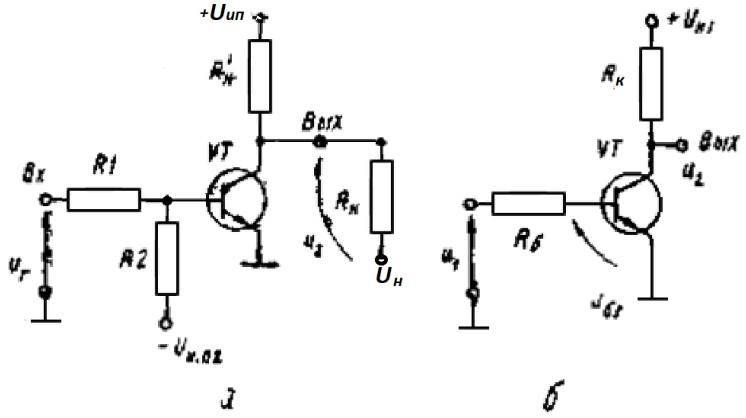


Fig.1.7

The bias source $-U_{un2}$ is not required if the transistor cutoff mode is provided by the low level of the input signal U^0_1 and the condition of closure is not disturbed at maximum ambient temperature.

To simplify the analysis of the statics and dynamics of such a switch, we transform the scheme using the equivalent generator theorem. The components of the transformed scheme (fig. 1.7-b) are determined from the relations:

$$U_{u1} = [U_{un.}R_н + U_н R'_к] / [R_н + R'_к],\ R_к = R'_к || R_н,\ U_1 = (U_г R_н + U_{un.2} R_1) / (R_н + R_1).$$

To provide the transistor cutoff mode, it is necessary that, at a low level U^0_1 of the input signal, the emitter junction of the transistor was locked. As can be seen from Fig. 1.5-*б*, locking can be considered low potential U^0_1 at the input, which provides on the emitter junction voltage $U_{бе} \le U_0$. If this condition is fulfilled, then both transistor junctions are locked and the transistor in the circuit of Fig. 1.7-*б* the first approximation can be replaced with the source of the reverse current of the collector junction $I_{к0}$ (Fig. 1.8-*а*).

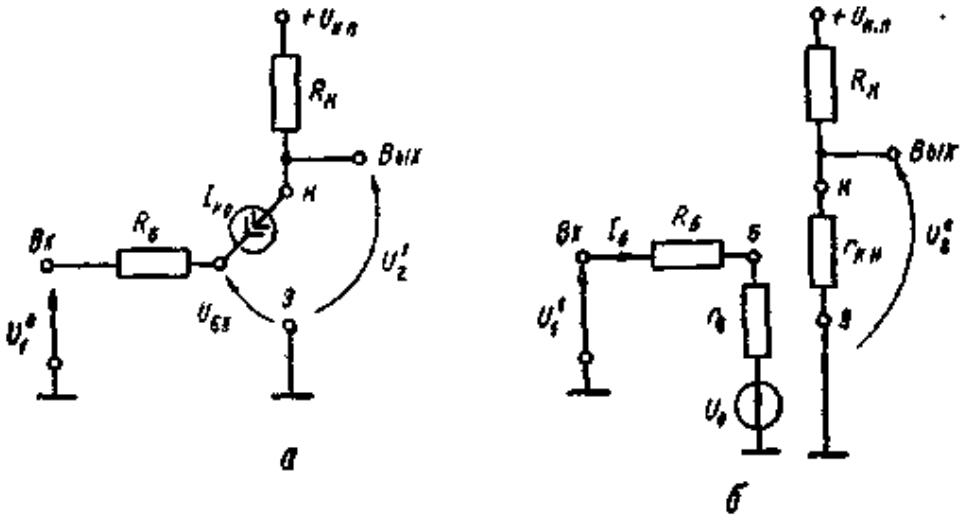


Fig. 1.8

The thermal current $I_{к0}$ flows through the resistor $R_б$ and increases the potential of the base. The higher the collector junction temperature, the greater the current I_{K0} and the voltage $U_{бе}$. The condition for locking the transistor must be performed in the worst case, that is, at the maximum temperature of the collector junction and the corresponding current $I_{к0max}$ through it:

$$U_{бе} = U^0_1 + I_{к0max} R_б \le U_{0,} \qquad (1.5)$$

If the condition (1.5) is satisfied, the transistor *VT* is locked; on its collector, which is the output of the circuit, a high level is set:

$$U^1_2 = U_{un} - I_{к0} R_к. \qquad (1.6)$$

To unlock the transistor, you must submit a high level $U^1_1 > U_0$, on input of the switch. In this case, the transistor can be in active mode or in saturation mode. The saturation mode occurs if the base current $I_б$ of the transistor, reaches or exceeds the $I_{бн}$ value, which corresponds to the position of the transistor operating point at the interface between the active mode and the saturation mode: $I_б \geq I_{б.н}$.

The input circuit of the saturated transistor in the linear approach version can be present in the same way as a diode by a series-connected volume impedance of the base $r_б$ and a voltage source U_0. The resistance between the collector and the emitter of the saturated transistor is determined by the slope of the saturation line (Fig. 1.5-*в*): $r_{кн} = \Delta U_{ке} / \Delta I_к$ when $I_б \geq I_{бн}$. An equivalent circuit of a transistor switch in saturation mode is shown in Fig. 1.8-*б*. For this scheme, the saturation condition has the form:

$$I_б = (U^1_1 - U_0) / (r_б + R_б) \geq I_{бн} = I_{кн} / \beta_{min} = U_{ип} / (\beta_{min}(R_к + r_{кн})), \qquad (1.7)$$

Since the gain of the current transistor β has a technological range, inequality (1.7) must be performed in the worst conditions, that is, with the smallest allowable value $\beta = \beta_{min}$. If the condition (1.7) is satisfied, the transistor *VT* is saturated and the low-level transistor is set at the output of the open switch:

$$U_2^0 = r_{кн}I_{кн} = r_{кн}U_{ип} /(R_к + r_{кн}).$$

1.3. Transition processes

The inertia of the switch based on the bipolar transistor is characterized by the duration of the switching cycle, which includes: $t_{зт.вкл}$.- delay of switching on the transistor when input of the switch by a high level signal U_1^1, which satisfies the condition (1.7); $t_{вкл}$ - the duration of the transistor's inclusion, that is, the time of the increase of current through the transistor from the thermal $I_{к0}$ to the saturation current $I_{к.н}$; $t_р$- the duration of the shutdown delay due to the recombination of charge in the base when the transistor passes from saturation to the active mode; $t_{викл}$- the time of the switching, that is, the reduction of the collector current of the transistor from the saturation current $I_{кн}$ to the current level $I_{к0}$; $t^{01}_ф$- duration of the potential increase on the collector of the transistor, due the charge capacities of loading and installation.

Then, the full cycle of switching or split time $T_{роз}$ is equal to the sum of the named intervals:

$$T_{роз} = t_{зт.вкл} + t_{вкл} + t_р + t^{01}_ф.$$

This is the time necessary to recharge the parasite capacitance of the circuit mounting, interelectrode capacitance of the transistor, to accumulate the charge of minority carriers at the base of the transistor at the offset and recombination of this charge when the transistor is locked.

Since the collector current of the bipolar transistor is a current of extraction of non-main charge (here - electrons) from the base and is proportional to the charge in the base, the transients are conveniently analyzed by the dynamics of charge changes. Therefore, such method of analysis of transients is named the method of analysis of charge of base.Fig.1.9

Fig 1.9-*а* shows the variant of the equivalent circuit (see fig. 1.7-*б*) of the transistor switch, which shows the load capacitance of $C_н$ and the equivalent input capacitance of the transistor $C_{вх}$, due to the capacitances of the emitter and collector junction of the transistor, as well as the parasitic capacitance of the installation.

Consider the characteristic sections of the transitional process in time diagrams (Fig. 1.9-*б*).

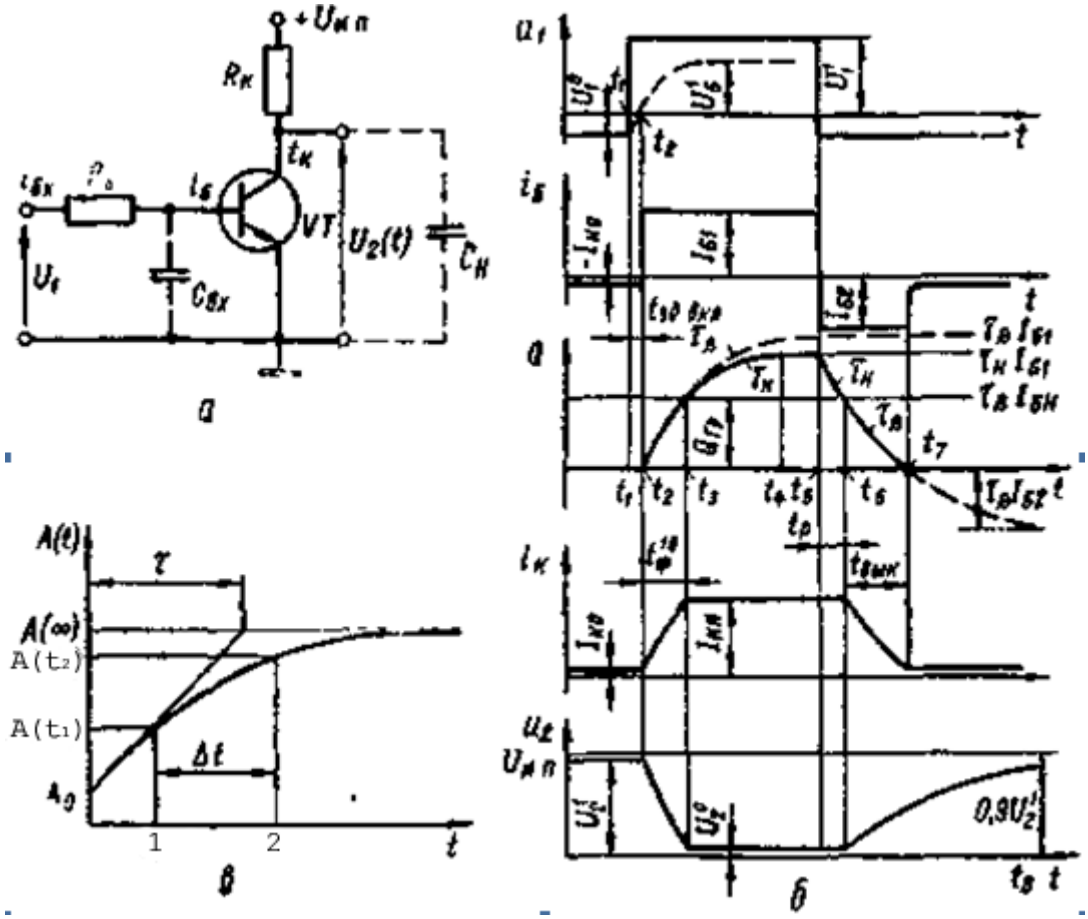


Fig. 1.9

1. By the time t_1, the transistor *VT* is locked at a low level of the input signal U^0_1, which satisfies condition (1.5). The current in the base circuit of the transistor is determined by the reverse current of the collector junction: $I_Б = -I_{к0}$. The charge Q of the base in the absence of injection of minority carriers through the emitter transition is practically absent: $Q \approx 0$. In the collector circuit, the return current of the collector transition is $I_к = I_{к0}$. At the switch output, a high level is maintained:

$$U^{1}_{2} = U_{un} - I_{к0}R_{к}.$$

2. At time t_1, the potential at the input of the switch jumps increases from U^{0}_{1} to U^{1}_{1}. The base potential of the transistor $U_б$ increases with charge capacitor $C_{вх}$ due to resistance $R_б$. The voltage $U_б$ increases with the exponential law with a constant time $\tau_б = R_б C_{вх}$ from the initial voltage $U^{0}_{Cвх} = U^{0}_{1} + R_б I_{к0}$ to the asymptotic level $U_{Cвх}(\infty) = U^{1}_{1} + R_б I_{к0}$. By the time t_2, until the voltage on the base remains less than the threshold voltage U_0, the transistor remains in the cutoff mode, the charge of the base, the potential and collector current are not changed. The time interval from t_1 to t_2, when the potential of the base $U_б$ (the voltage at the emitter junction $U_{бе}$) reaches the threshold voltage U_0, determines the duration of the delay of the transistor activation, $t_{зт.вкл} = t_2 - t_1$. To determine the duration of the $t_{зт.вкл}$, we use the property of the exponential function (Fig. 1.9-*в*) $A(t) = A_0 + (A_\infty - A_0)(e^{-t/\tau} - 1)$, which is as follows: if the parameters of the exponential function $A\infty$ - is the asymptotic value, τ is the time constant, $A(t_1)$ and $A(t_2)$ are the exponential levels, the interval of time from t_1 to t_2 is determined by the relation:

$$\Delta t = t_2 - t_1 = \tau \ln[(A\infty - A\{t_1\})/(A\infty - A\{t_2\})]. \qquad (1.8)$$

Using this expression, we define the delay time for inclusion:

$$t_{зд.вкл} = \tau_б \ln[(U^{1}_{1} + I_{к0}R_б - \{U^{0}_{1} + I_{к0}R_б\})/(U^{1}_{1} + I_{к0}R_б - U_0)] \approx$$

$$\approx R_б C_{вх} \ln[(U^{1}_{1} - U^{0}_{1})/(U^{1}_{1} - U_0)]. \qquad (1.9)$$

3. At time t_2, the potential of the base exceeds the threshold voltage U_0, opens the emitter junction, and the transistor switches from the cutoff mode to the active mode. Injecting non-main charges into the base by the emitter (in the n-p-n-transistor they are electrons, and in p-n-p - holes) due accumulate charges in base. The rate of charge accumulation is higher, the larger the current of the base $I_б(t)$. With a sufficiently large base current, the input circuit of the transistor can be represented as Fig.1.8-*б*. Then the current in the open base transistor base circuit:

$$i_б(t) = (U_1(t) - U_0)/(R_б + r_б).$$

The increment of the charge of minority carriers ΔQ per unit time in the interval Δt is determined by the expression:

$$\Delta Q/\Delta t = i_б(t) - Q/\tau_{\beta}, \qquad (1.10)$$

where τ_β is the average lifetime of non-main charges. In expression (1.10), the first term describes an increase in the charge in the base (if $I_б(t) > 0$), and the second one is the decrease in charge due to the finite lifetime of non-main

charges τ_β and the recombination of a portion of the carriers in the active base region.

In the limit for infinitesimal intervals of time we obtain the differential equation of the first order:

$$dQ/dt = i_б(t)-Q/\tau_\beta , \qquad (1.11)$$

If $U_1(t) = U^1_1 = const$, the current of the transistor base remains practically constant:

$$i_б(t) = I_{б1} = (U^1_1-U_0)/(R_б+r_б) \approx U^1_1/R_б.$$

then the solution of equation (1.11) is an exponential function:

$$Q(t) = Q_1[1-exp(-t/\tau_\beta)]+Q_0 , \qquad (1.12)$$

where $$Q_1 = \tau_\beta I_{б1}, \qquad (1.13)$$

With the accumulation of charge in the base proportionally increases the collector current, the voltage drop on the resistor $R_к$ increases and the collector's potential falls. At time t_3 the transistor switches from the active mode to saturation mode, the collector current growth (see Fig 1.9) stops at the $I_{кн} = U_{дж.ж}/ (R_к + r_{к.н})$ and the collector potential falls at U^0_2 level.

The interval from the moment t_2 to $t_3$presents the switching time of the transistor $t_{вкл}$. Its duration can be determined using (1.12), if we take into account that the charge on this interval increases from $Q_0 = 0$ to the value

$$Q_{гр} = \tau_\beta I_{бн}, \qquad (1.14)$$

which corresponds to the position of the operating point of the transistor on the boundary between the active mode and the saturation mode. In this case, the charge increases exponentially with a constant time τ_β and asymptotically approached to the Q_1 level. Then, using the expression (1.8) and taking into account the formulas (1.13), (1.14) we obtain:

$$t_{вкл.} = \tau_\beta ln[Q_1/(Q_1-Q_{гр})] = \tau_\beta ln[(\tau_\beta I_{б1})/(\tau_\beta I_{б1}- \tau_\beta I_{б.н.})] = \tau_\beta ln[S/(S-1)] , \quad (1.15)$$

where $S = I_{б1}/ I_{бн}$- saturation coefficient of the transistor.

The duration of the front edge of the output signal is $t^{10}_ф \approx t_{вкл}$.

4. At this stage, all currents and voltages established at time $t_3$remain constant. The transition process is characterized only by the continued accumulation of charge in the base beyond the limit value of $Q_{гр}$. The charge of non-main carriers exceeding the value of $Q_{гр}$ is called excess. The charge continues to increase in exponentiation, but with a changed exponential parameter $\tau_н = 0,7$

... *1,5* τ_β, which characterizes the average lifetime of non-main charges in saturated mode. The change in the average lifetime of non-main charges is due to the redistribution of charge in the active base region when the transistor passes from the active mode to saturation. In this case, for fusion transistors, $\tau_н < \tau_\beta$, and for diffusion $\tau_н > \tau_\beta$. It can be assumed that at the time $t_н = 3\tau_н$the process of accumulation of excess charge $Q_{надл}$ ends and the charge reaches the value:

$$Q_2 = Q_{гр} + Q_{надл} = \tau_н I_{б1} \qquad (1.16)$$

The ratio of the accumulated charge Q_2 to the limiting $Q_{гр}$ in terms of expressions (1.14) and (1.16) approximates the saturation coefficient of the transistor:

$$Q_2/Q_{гр} = \tau_н I_{б1}/\tau_\beta I_{б.н.} \approx S \ .$$

5. At the rear *edge* of the input signal at time t_5, the current of the base $I_б(t)$ of the transistor jumps varies by magnitude (and sign) $I_{б2} = (U^0{}_1 - U_0) / (R_б + r_б)$, the equilibrium state of charge of the base is violated and its recombination begins. The excess charge exponentially with a constant time $\tau_н$ decreases from the value Q_2, seeking asymptotically to $Q_3 = \tau_н I_{б2}$. At this stage, the charge in the base $Q(t) > Q_{гр}$ and the transistor remains saturated until t_6 when the excess charge recombination ends and the saturation transistor enters to the active mode. In the interval from t_5 to t_6 the collector current $I_к$and the output voltage U_2 remain unchanged, and this stage of the transition process is called the recombination time. Duration of the stage of recombination:

$$t_p = t_6 - t_5 = \tau_н ln[(Q_3 - Q_2)/(Q_3 - Q_{гр})] = \tau_н ln[(I_{б2}\tau_н - I_{б1}\tau_н)/(I_{б2}\tau_н - I_{б.н.}\tau_\beta)] \approx$$
$$\approx \tau_н ln[(_{Sзап} - S)/(S_{зап} - 1)] \ , \qquad (1.17)$$

where $I_{б2}/I_{бн} = S_{зап}$ - the coefficient of closure.

6. At time t_6 the transistor enters the active mode and from the level $Q_{гр}$ the base charge exponentially with the constant time τ_β decreases, seeking asymptotically to $Q_4 = \tau_\beta I_{б2}$. At the same time synchronously decreases the current collector $I_к$ and begins to increase the output voltage. This stage, which is called the exclusion stage, ends at time t_7, when the level $Q\ (t) \approx 0$is reached. Duration of the exclusion stage:

$$t_{викл} = t_7 - t_6 = \tau_\beta ln[(Q_4 - Q_{гр})/Q_4] = \tau_\beta ln[(I_{б2}\tau_\beta - I_{бн}\tau_\beta)/I_{б2}\tau_\beta]$$
$$= \tau_\beta ln[(S_{зам} - 1/S_{зам}]. \qquad (1.18)$$

At time t_7, the transistor goes into the cutoff mode, its input impedance sharp increases, the base current is set to $I_б\ (t) = -I_{к0}$, and the collector current is $I_К\ (t) = I_{к0}$.

7. The increase in the output voltage $U_2(t)$ is associated with the charge due to the collector resistance of $R_к$ of the equivalent load capacity $C_0 = C_н + C_{к..б}$. +

$C_м$, where $C_н$, $C_{к.б}$, $C_м$ - capacity of a load, collector's transition and installation. The duration of the rear front is $t^{01}ф \approx 3\tau_{зар} = 3R_кC_0$. In the case of a purely active load and a small installation capacity ($C_м \approx 0$), $t^{01}ф \approx t_{викл}$ can be considered.

Analyzing the dependence of the duration of the time $t_{роз}$ difference of the transistor switch on the parameters of its components and control signals, we can draw the following conclusions: the time $t_{роз}$ less, then the less the $\tau_β$ of the transistor, that is, the greater the marginal amplification frequency $f_α=(β+1)/(2πτ_β)$; with increasing transistor saturation coefficient, the duration time $t_{вкл}$ decreases, the time of recombination t_p increases, and the duration of the exclusion $t_{викл}$ does not change, the recombination time t_p and the time of the exclusion $t_{викл}$ the smaller the bigger factor of the $S_{ЗАМ}$.

Therefore, the minimum duration of the $t_{доз}$ can be obtained using transistors of the required frequency range and the optimal choice of signal levels controlled by the switch U^0_1 and U^1_1. If, however, the minimum $t_{доз}$ is more than permissible, it is necessary to use circuit technical methods of forcing transients in transistor switches.

1.4. The switch based on a bipolar transistor with a nonlinear feedback

The duration of the switch-on phase of the transistor $t_{вкл}$ can be reduced by supplying a larger discharge current to the base. In accordance with the expression (1.15), the $t_{вкл}$is decreasing, but due to the growth of the saturation coefficient S, the duration of the resorption phase t_p increases simultaneously. As a result, in spite of additional power losses, the speed of the switch is not increased. One of the outputs in this situation is the exclusion of the saturation mode of the transistor and thus the switching of its operating point between the active mode and the cut-off mode.

In Fig. 1.10. (*a*) is shown a schematic diagram of a transistor switch that uses a nonlinear feedback (NLF) via a *VD* diode (parallel negative feedback voltage). The depth of such an NLF depends on the mode of the diode: if the diode *VD* is locked, the influence of feedback on the operation of the switch can be neglected. If the *VD* diode is open, then due to its low resistance $r_д$the deep feedback and the voltage transfer coefficient in the circuit are realized:

$$K_u^{o.c.} = U_2/U_1 \approx r_д/R_б \text{ -> } 0\ , \qquad r_д << R_б$$

and the potential of the collector of the transistor is fixed.

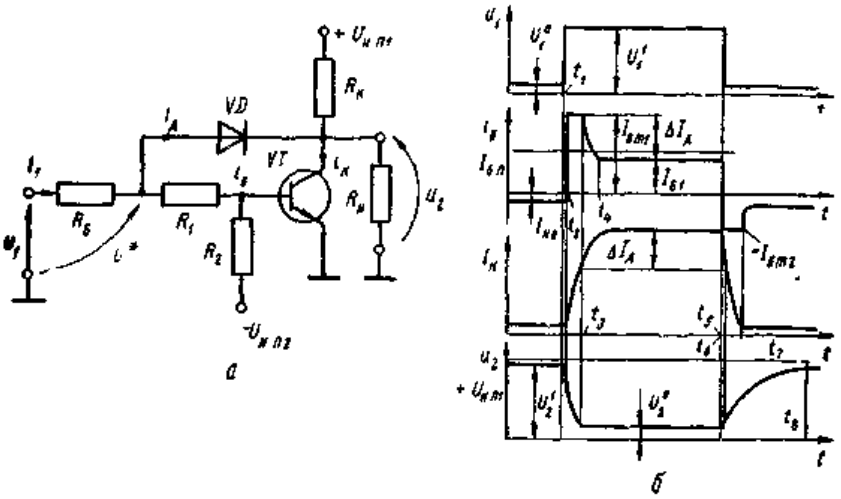


Fig.1.10

In Fig. 1.10 (б) shown time transient diagrams when applying the positive pulse switch to the input. Before the time t_1 at the switch input there is a low level of U^0_1 signal, the transistor *VT* is closed, on its collector is supported by high potential U^1_2, which causes the inverse displacement of the diode *VD*. At time t_1, the input sharp increases from zero U^0_1 to the unit level U^1_1. Through $t_{зт.вкл}$ at the moment t_2 opens the emitter transition and the base of the transistor sets the current of the base:

$$I_{бm1} = [U^1_1 R_2 - U_{u.n2}(R_б + R_1) - U_0(R_б + R_1 + R_2)]/B,$$

where $B = R_б R_2 + R_1 R_2 + R_2 r_б + r_б R_1 + R_б r_б$, $r_б << R_1, R_2, R_б$.

As the collector current increases, the potential of the collector U_2 falls, while the closing voltage on the diode VD decreases:

$$U_д = U^* - U_2 = U_0 + I_{бm1} r_б + I_{1m} R_1 - U_2$$

where $I_{1m} = [U^1_1(R_2 + r_б)/(B - R_2 r_б)] + [(U_{u.n2} r_б - U_0 R_2)/B] \approx [U^1_1/(R_б + R_1)]$ - the input current until the diode is unlocked.

At the time t_3, when the collector potential is close to the saturation voltage, the *VD* diode opens and the input current I_{1m} is redistributed between the *VD* diode and the resistor R_1: the current of the resistor R_1 is reduced by the magnitude of the diode current increase $\Delta I_д$. Since the current of the diode closes through the collector circuit of the transistor at a practically constant collector potential, then the collector current from the moment t_3 increases by an amount of $\Delta I_д$. The potential of the collector of the open transistor differs from the potential U^* by the value of the voltage on the open diode. If we take it equal to the threshold voltage $U_{од}$ of the diode, then approximate (since the small change in voltage U^* after disconnecting the diode is not taken) voltage at the output:

$$U^0_2 = U^* - U_{од} = U_0 + I_{бm1} r_б + I_{1m} R_1 - U_{0д}$$

At time t_4, the constant values of the currents of the base $I_{б1}$, $I_{1к}$ collector and diode are set.

On the back edge of the input signal is current through a diode changed to the opposite direction, its return resistance is restored and until t_6 the diode is turned off. Thus, the NFL breaks apart and a recombination of the charge in the base of the current begins:

$$I_{бm2} = [U^0_1 R_2 - U_{u.n2}(R_б + R_1) - U_0(R_б + R_1 + R_2)]/B.$$

Further, the transient processes in the switches with NLF are similar to those previously considered in the transistor switch (see Fig 1.9).

In the scheme under consideration, there is no shutdown delay due to the excess charge of the base of the transistor, but there is a process of recombination of the charges accumulated in the diode. Therefore, in practice for the implementation of NLF choose high-speed pulsed diodes or Schottky diodes that operate without charge.

The duration of the stages of switching on and off the transistor in the circuit with the NLF is determined by the disconnecting $I_{бm1}$ and the closing $I_{бm2}$ base currents, which, in turn, depend on the resistance of the resistors R_6, *R1*, *R2* and the voltage levels U^0_1, U^1_1, $U_{un.2}$.

Output voltage U^0_2 also depends on the parameters of the input signal, which in the switching circuits is undesirable. The circuit in which the resistor *R1* is replaced by the *VD2* diode is shown in Fig. 1.11-*а*. In this scheme, when unlocking the diodes *VD1* and *VD2* on the transistor collector, the potential is fixed:

$$U^0_2 \approx U_0 + U_{0д2} - U_{0д1} \approx U_0,$$

where U_0 is the threshold voltage of the transistor, $U_{0д1}$ and $U_{0д2}$- the threshold voltages of the diodes *VD1* and *VD2*, respectively. Voltage U^0_2 slightly exceeds the voltage on the saturated transistor and does not depend on the parameters of the input signal.

If a *Schottky* diode is used as a diode *VD1*, which has a very small threshold voltage $U_{0ш} \approx 0.1$ *V*, then the *VD2* diode in the base of the transistor circuit is not required (Fig. 1.11-*б*), the *Schottky* diode and the collector junction of transistor are included in parallel, but due to the fact that the limiting voltage of the diode $U_{0ш}$ is essentially less than the threshold voltage of the collector junction (for the silicon transistor $U_{0к} \approx 0{,}5 \ldots 0{,}7$ *V*), the *Schottky* diode opens earlier and thus prevents the transistor saturation.

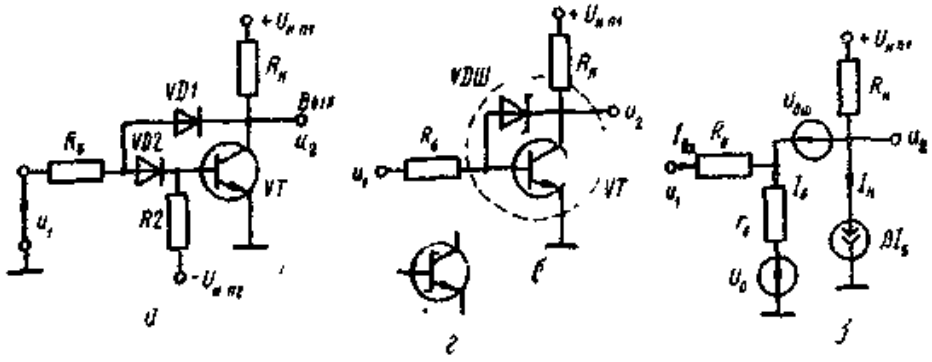


Fig.1.11

In the open state, the potential of U^0_2 is determined on the transistor collector, which can be determined by an equivalent switch circuit (Fig. 1.11-*в*):

$$U^0_2 = I_б r_б + U_0 + U_{0ш}.$$

Voltage U^0_2 is small (about 0.1 V), practically does not depend on the input signal and resistance in the base circuit and collector circuit. Another important advantage of the circuit (Fig 1.11-*б*) is its high speed, the *Schottky* diode works without accumulation of charge, so there is no stage for restoring the feedback resistance of the diode. The advantages of a transistor with a collector-base connection through a *Schottky* diode have led to the creation of a monolithic structure of a diode, a *Schottky*-bipolar transistor manufactured in a single technological process, called the *Schottky* transistor (Fig. 1.11-*г*) and is widely used in integrated circuit engineering.

1.5. Electronic switches based on field effect transistors (FET)

For construction of electronic switches, it is possible to use field effect transistors with p-n-junction control, with an isolated switch and a built-in or induced channel. In the digital circuitry, Metal Oxide Semiconductor Field Effect Transistor (MOSFET) with induced p- or n-channel have become the most widely used.

In Fig. 1.12 *в* -shows the graphic image of a n-type inductive MOS transistor.

In Fig. 1.12-*а, -б* shows the drain and gate I–V curve of the MOS -transistor with induced n-channel. If the voltage $U_{з.с} < U_{пор}$, then the charge transfer channel is not induced and the transistor is locked. If $U_{з.с} > U_{пор}$, then the n-channel is induced in the sublingual region, through which the current flows, which is determined by the voltage $U_{с.и}$ between the channel electrodes, the transistor is open and its working point is in the steep (triode, I) or gently sloping (pentode, II) characteristics area. Accordingly, in the field of characteristics I or II, the drain current of the transistor i_c is described by the expressions:

$$\text{I: } i_c = \mu[(U_{зи} - U_{пор})U_{с.и} - 0{,}5U^2_{с.и}] \ ,$$

II: $i_c=0{,}5\mu\,(U_{зи}-U_{пор})^2$,

where μ is the specific steepness of the control characteristic, the $U_{пор}$ -threshold voltage of the current cutoff.

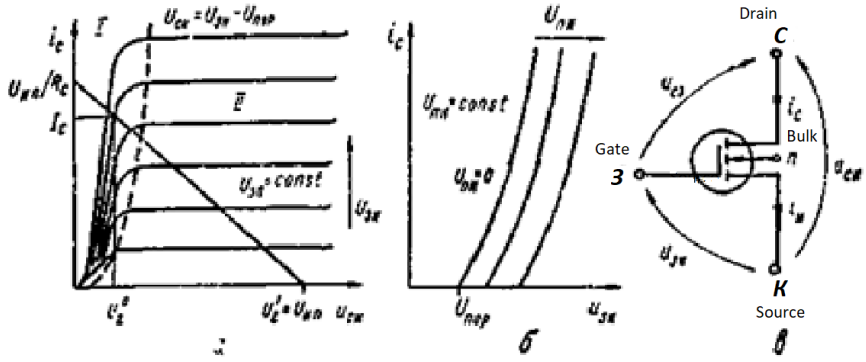


Fig. 1.12

In Fig. 1.13-*а* is a diagram of the simplest switch on the MOS transistor, included in the scheme with a general leakage and with the linear stock load R_c. If the load of the switch is an active resistance of $R_н$, it can, by using the equations for the equivalent generator, be included in the equivalent resistance R_c.

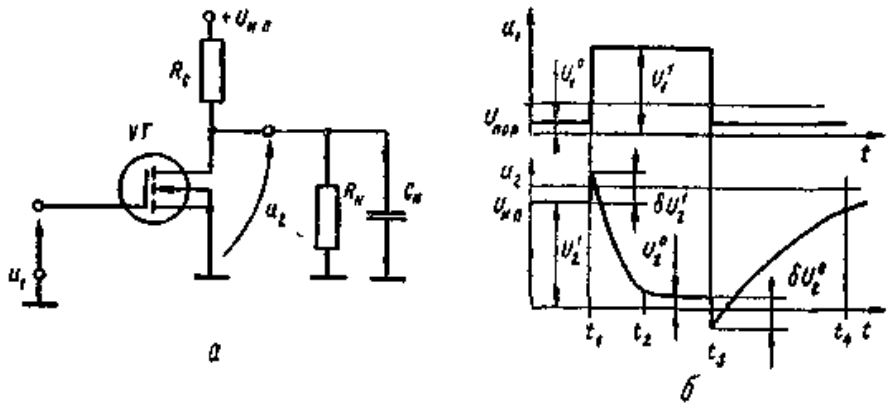


Fig. 1.13

The static mode of such a switch is determined by the loading line on the family of stock characteristics (Fig. 1.12-*а*). At low level of the input signal $U^0{}_1<U_{пор}$ the MOS transistor is in the cutoff mode and, since the leakage current through the closed channel I_c is sufficiently small ($I_c<10^{-9}$ *A*), it is possible to assume the high level of the output signal $U^1{}_2= U_{u.n}$. The power consumption from the power source U_{un} in the closed state of the switch is $P^1{}_{nom} = 0$. At a high level of the input signal $U^1{}_1 >U_{пор}$ in the transistor, the channel is induced and the current $I^1{}_c$ flows through it, which is determined by the point of intersection of the loading line with the stock

characteristic $i_c = f(U_{сн})$. Depending on the value of the input voltage U_1, the supply voltage $U_{u.n}$ and the resistance R_c, the working point of the transistor is detected in the "triode" region (the steep areas of the flow characteristics), to the left of the line, which is the geometric location of points of overlap of the flow characteristics (area I in fig. 1.12-*а*), or in "pentode" (area II grate areas in fig 1.12-*а*), to the right of the line (1.19):

$$U_{сн} = U_{зи} - U_{пор}. \qquad (1.19)$$

At the output of the switch is set low potential:

$$U^0_2 = U_{ип} - I_c R_c\ , \qquad (1.20)$$

where I_c - flow current, which is defined graphically from Fig. 1.12-*а*.

To solve the analytical determination of the operating point of the open transistor ($U_{с.и} = U^0_2$, $i_c = I_c$), one must solve the equation (1.20) and one of the approximating stock characteristics of the equations for the triode region: $i_c = \mu\,[(U_{зи}-U_{пор})U_{сн}-0{,}5\,U^2_{си}]$or for the pentode area: $i_c = 0{,}5\mu(U_{з.и}-U_{пор})^2$where μ is the specific steepness of the drain and gate characteristic.

The transients processes in the switches on the field transistors are due to the transfer of carriers with mobility v through the length L channel and the recharge of the inter electrode capacitances of the transistor (drain –bulk $C_{С3}$, drain - source $C_{Cи}$), as well as the load capacities of the $C_н$ and the parasitic capacitance of the installation $C_м$.

The transport time of carriers through the channel $t_{пер} = 2{,}2L^2/(vU_{с.и})$, where for electrons the mobility $v_n = 0{,}04\ м^2/(Vs)$, and for holes - $v_p = 0{,}02\ м^2/(Vs)$, so n-channel MOS transistors have higher performance. At length of channel L the order of units of microns and voltage $U_{с.н}$ of order of tens volt $t_{пер}$ is very small and has the order of $10^{-9}s$. Therefore, the speed of the switches on the MOS-transistors determined with processes of recharging of the interelectrode and external capacitances of the transistor.

In Fig.1.13-*б* - show the timing diagram of the idealized input signal $U_1(t)$and the output signal $U_2(t)$. The jump of the input signal at time t_1 causes the in-phase interference δU^1_2 at the output due to the transfer of the input part directly to the output through the capacitive voltage divider from the capacitance $C_{с.з}$ and capacitance C_0, which includes the capacity drain - source $C_{с.и}$, the load capacity $C_н$ and assembling$C_м$

$$\delta U^1_2 = [(U^1_1-U^0_1)C_{с.з}]/[\,C_{с.з}+ C_0],$$

where $C_0 = C_{с.и}+C_м+C_н$.

Further, the capacitance C_0 is discharged, and the capacitance $C_{сз}$ is recharged through the open transistor and the drain resistor R_c. In general, the speed of the process at this stage is determined by the conductivity of the open transistor, the output voltage exponentially falls with a constant discharge time:

$$\tau_p = [(C_0+C_{с.з})R_c]/[\mu(U_{и.п}-U_{пор})R_c+1] \; . \qquad (1.21)$$

Then the duration of the negative edge of the output signal (the time interval from t_1 to t_2 when the signal drops by $0.9\ (U^1_2-U^0_2)$) can be estimated as:

$$t^{10}_{Ф} \approx 3\tau_p = [3(C_0+C_{с.з})]/[\mu(U_{и.п}-U_{пор})].$$

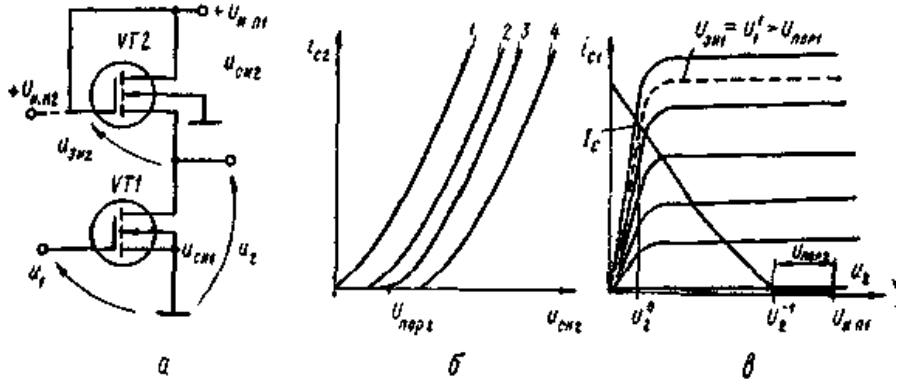


Fig.1.14

At the back edge of the input signal at the moment t_3, the common-mode emission $\delta U^0_2 = \delta U^1_2$ is formed. Then the transistor is rapidly closed (in time of nanoseconds), and the charge of the equivalent capacitance C_0 and the recharge of the capacitance $C_{с.з}$, which proceeds according to the exponential law with constant charge time, proceeds: $\tau_з = (C_0+C_{с.з})R_c$. Accordingly, the duration of the positive edge of the output signal is $t^{01}_{Ф} \approx 3\tau_з = 3R_c(C_0+C_{с.з})$.

From the standpoint of integral technology, the switch under consideration has significant disadvantages: it is difficult to produce transistors and high-resistance (drain -R_c) resistors in a single technological cycle. Except is high-energy consumption in the open state $P^0_{пот} = U^2_{и.п}/R_c$.

The first of the disadvantages is eliminated in the integrated circuits by replacing the linear resistor R_c with a nonlinear one, which uses the MOS transistor with bipolar inclusion (Fig. 1.14-*а*) with a shorted bulk and drain. For transistor *VT2:* $U_{сн2} = U_{зс2}$. If on the family of drain characteristics of the transistor *VT2* to construct an infinite line dividing the pentode and triode regions (Fig. 1.14-*б*- curve 1) for which the expression is correct (1.19) and shift it along the axis of voltage to the value of the $U_{пор}$, we obtain a nonlinear dependence - I–V curve of the MOS-transistor in bipolar inclusion (Fig.1.14-b - curve 3). In the same graph, the I–V curve loading transistor *VT2* is given at the supply of an arbitrary constant voltage $U_{и.п2}$ to its switch (curve 2 - if $U_{и.н1}<U_{и.н.2}< U_{и.н.2}+U_{пор}$, curve 4 - if $U_{и.н2}<U_{и.н1}$). In order to

provide I–V curves close to the linear, as transducers, transistors with a low specific steepness shut-off characteristic μ and a minimum voltage $U_{пор2}$ are manufactured as a load.

We construct the I–V curve of a nonlinear two-terminal on the family of flow characteristics of the switching transistor *VT1* as a line of its load (Fig 1.14-*в*). This allows you to graphically determine the levels of the output voltage of the switch in the locked U^1_2 and the open U^0_2 state, as well as the current of the open transistor *VT1* with the load *VT2*. Note that in the closed state, when both transistors are closed, the high level U^1_2 is not defined strictly, since it depends on the random resistance of the leakage of the transistors *VT1* and *VT2*:

$$U^1_2 = U_{u.n.1}\, R_{вит.1}/(R_{вит.1}+R_{вит.2})$$

and may vary in the range $U_{u.n1} > U^1_2 > U_{u.n1}-U_{пор.2}$.

The considered circuit scheme is more technological for integrated circuitry, but it has high consumption of $P^0_{nom} = U_{u.n1}I_c$ when the transistor *VT1* is open. Reducing the power of P_{nom} by simply increasing the R_c resistance can only be made to certain limits, which are determined by the ratios for the maximum permissible length of the fronts $t^{10}_{ф}$ and $t^{01}_{ф}$. Significantly, the power consumption of an electronic switch can be reduced if, as a load, use an element with a controlled internal impedance, which when closing the transistor *VT1* should have minimum resistance, and when unlocking - the maximum.

In the scheme in Fig. 1.15-*а* as a load of the n-channel transistor *VT1* used p-channel transistor *VT2*, controlled by the direct input signal U_1. Due to the symmetry of the circuit, each of the transistors is a controllable load for another transistor. Different types of conductivity when operating with the same signal U_1 provide mutually opposite modes of operation. Therefore, it is said that the transistors in this scheme complement each other one, they form the so-called complementary structure.

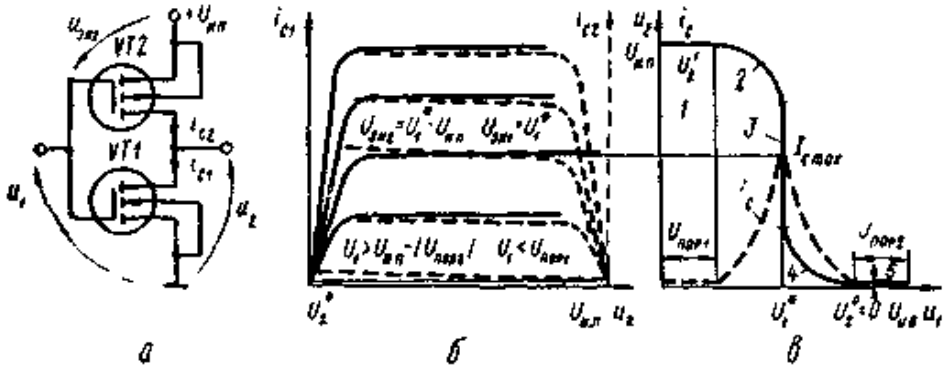


Fig. 1.15

The type of static transfer characteristic of the complementary structure depends on the ratio of the supply voltage $U_{u.n}$and the threshold voltages of the n-channel ($U_{nop.1}$) and p-channel ($U_{nop.2}$) transistors. If $U_{u.n} > U_{nop.1} + |U_{nop.2}|$, then the transfer characteristic (Fig. 1.15-*в*) contains the following characteristic areas.

1. $U_{зс1} = U_1 < U_{nop.1}$- Transistor *VT1* in the cutoff mode, $|U_{зс2}| = |U_1 - U_{u.n}| >> |U_{nop.2}|$ - transistor *VT2* in triode mode. Output voltage is defined as the result of the voltage supplied between the high resistor of the leakage of the locked transistor *VT1* $R_{вит} = 10^9 ... 1\ 0^{12}$ Ω and the small resistance *VT2* in the triode mode $r^T_{i2} \sim 10^2$ Ω, so the output level is set to $U^1_2 = [U_{u.n} R_{вит.1}] / [R_{вит.1} + r^T_{i2}] \approx U_{u.n}$. Typical value of high level $U^1_2 = 0.999 U_{u.n}$. The current consumed from the power supply is insignificant: $I^1_{пот} = U_{u.n} / [R_{вит.1} + r^T_{i2}] \approx U_{u.n} / R_{вит.1}$.

2. $U_{п.т.1} < U_1 < U_{п.т.2}$; $U_{п.т.2}$- the limiting voltage of transistor transition VT2 from the triode mode to pentode. In this area, VT1 works in pentode, and VT2 - in the triode of characteristics. The complement pair is in amplification mode with the voltage transfer factor $K_U = -\mu_1 \cdot (U_{nop} - U_1) \cdot r^T_{i2}$, where r^T_{i2} is the differential resistance of the *VT2* transistor in triode mode, μ_1 is the specific steepness of the control characteristic of the transistor *VT1*. K_U is insignificant because $r^T_{i2} << r^п_{i2}$. Current$I_{пот}$through transistors is increasing.

3. $U_{п.т.2} < U_1 < U_{п.т.1}$, $U_{п.т.1}$ - the limiting voltage transition of the transistor VT1 from the pentode mode to the triode. Both transistors are in pentode mode and provide the maximum voltage transfer factor $K_U = -(\mu_1 + \mu_2) \cdot (U_{nop} - U_1) \cdot [r^n_{i1} \,||\, r^n_{i2}]$. Consumption current continues to grow to the middle of area 3 to the value $I_{C1} = I_{C2} = I_{Cmax}$(fig 1.15-*б*, -*в*) and then with increasing U_1 the consumption current begins to decrease, as the transistor *VT2* from the value $U_1 = 0{,}5 U_{u.n}$ closes faster than opens *VT1*.

4. $U_{сп.т.1} \le U_1 < U_{u.n}$. -| $U_{nop.2}$ |°- the transistor *VT1* from the pentode goes into the triode mode, and *VT2* remains in the pentode. The transmission coefficient of the voltage is less than in the region 3, $K_U = -\mu_2 \cdot (U_{nop} - U_1) \cdot [r^т_{i1}][r^n_{i2}]$and with the growth of U_1 decreases as the differential resistance $r^т_{i1}$ of the transistor *VT1* in the triode mode decreases. The current consumption of $I_{пот}$ is reduced due to the locking of the transistor *VT2*.

5. $U_1 > U_{u.n}$- | $U_{nop.2}$ |°- the transistor *VT1* is in triode mode, the transistor *VT2* - in the cutoff mode and because of its resistance to the flow of $R_{вит.2}$flows a very small current. Output voltage of the switch $U^0_2 = [U_{u.n} r^т_{i1}] / [R_{вит.2} + r^т_{i1}] \approx 0$. The typical low output level $U^0_2 = 10^{-3} U_{u.n}$. The power consumption current is negligible:

$$I^0_{пот} = U_{и.п.}/(R_{вит.2}+r^т_{i1}) \approx U_{и.п.}/R_{вит.2}.$$

When using a power source $U_{и.п} < U_{пор} + |U_{пор2}|$ regions 2, 3, 4 of the transfer characteristic (Fig 1.15-*в*) are merged and remain only areas 1 and 5, for which all of the above is fair. A zone of overlapping of region 1 and 5 appears, in which both transistors are in cut-off mode and the level of the output signal is determined by the leakage resistance of the closed transistors:

$$U_2 = U_{и.п.}R_{вит.1}/(R_{вит.1}+R_{вит.2}),$$

With $R_{вит.1}$ and $R_{вит.2}$varying in fairly wide limits by chance law. Uncertainty in the overlap area is eliminated when an external load is connected.

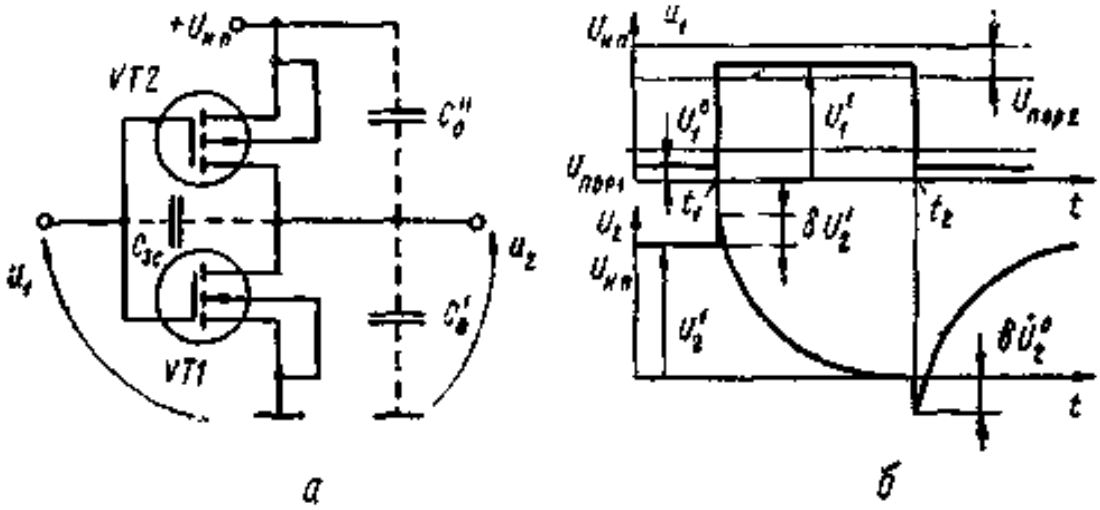


Fig.1.16

Transient processes in the switch on complementary MOS transistors are determined by recharging the interelectrode capacitances of the transistors *VT1*, *VT2*, as well as the capacitance of the load $C_н$ and the parasitic capacitance of the mounting $C_м$ (Fig. 1.16-*б*).

Suppose that by the time $t_1 U_l = U^0_1 < U_{пор.1}$. Then transistor *VT1* is closed, and *VT2* - in triode mode. At the output of the switch we have a high signal level $U^1_2 = U_{и.п}$, the capacities $C'_н$, $C'_м$, $C'_{св}$ are charged, and $C''_н$, $C''_м$, $C''_{св}$ - discharged. The incoming input signal U_1 at time $t_1$causes an in-phase output jump:

$$\delta U^1_2 = [(U^1_1 - U^0_1)C_{с.з}]/(C'_0+C''_0), \qquad (1.22)$$

where $C_{с.з} = C_{с.з.1}+C_{с.з.2}$, $C'_0 = C_{с.и.1}+C'_м+C'_н$, $C''_0 = C_{с.и.2}+C''_м+C''_н$. If $U^1_1 > U_{и.п.} - |U_{пор.2}|$, the transistor VT2 turns out to be closed, and VT1 is open and its operating point as the output potential decreases, it moves from the pentode region to the triode. The rate of increasing of the output voltage is determined by the discharging of the

capacitance C'_0, the charging C''_0 and the recharging of the capacitance $C_{c.з}$through the open transistor VT1, the differential resistance of which $r_{i1}$and with the decrease of the potential U_2 also decreases. Therefore, the change function $U_2(t)$ in Fig. 1.16-*б* is practically no different from the exponential and the duration of the negative edge of the output signal can be determined using the relation:

$$t^{10}_{ф} \approx 3\tau^{10} = 3C\, r^{т}_{i1}, \quad (1.23)$$

where $C = C'_0 + C''_0 + C_{з.с}$, $r^{т}_{i1}$- differential resistance of the drain of the transistor *VT1*.

At the back edge of the input signal at the moment $t_2$at the output of the switch is also formed a single-phase obstacle δU_2, which amplitude is determined from equation (1.22). Transistor *VT1* goes into cutoff mode, transistor *VT2* - first in pentode and then with increasing output voltage U_2 (voltage reduction $U_{с.в.2} = U_2 – U_{u.n}$), in triode mode. The positive front of the output signal is also formed by law close to the exponential and is determined by the relation:

$$t^{10}_{ф} \approx 3\tau^{01} = 3C\, r^{T}_{i2}. \quad (1.24)$$

The current consumption i_{nom} (t) is also related to the recharging of the equivalent capacitance *C*, since the through-current through both transistors can be ignored when practically instantaneous closing one of them.

The switches by complementary MOS transistors (CMOST) provide high-speed performance with rather insignificant power consumption, which depends on the switching frequency. They provide maximum power consumption $(U^1_2 - U^0_2 \approx U_{u.n})$ and keep operating in a wide range of voltage supply: $U_{u.n} = 3...15V$. Lowest power consumption is characterized by the switches that are fed from the voltage source $U_{u.n} < U_{nop.1} + | U_{nop.2} |$, in which the active component of the consumption current in the static mode is $I_{nom.a} = 0$. Low power consumption allows the use of the switches on the CMOST as the basic elements of integrated circuits with a high degree of integration.

The mentioned advantages of such switch schemes are achieved by complication of technology of their manufacture and increase in cost, but as the technology of integrated microcircuit technology is improved, these disadvantages are becoming less significant.

2. Diode-transistor logic elements (DTL)

Elements such as diode transistor logic (DTL) have been widely used since the mid-sixties of the twentieth century, thanks to the simplicity of schemes, the flexibility of expanding functionality (combining outputs in the assembling OR, increasing the number of inputs by connecting external diodes, etc.). Competitive technologies have pushed DTL elements due to higher performance, reduced power consumption and improved other operating parameters. However, the use of

Schottky's high-speed diodes in DTL-elements significantly increased their performance and increased the interest of developers in the corresponding series of integrated circuits.

2.1. The basic element of the NAND (Sheffer-element)

Consider the diode-transistor element NAND (Fig 2.1). The scheme of the element contains the following functional parts:

• diode logic circuit AND with two inputs (*R1, VD1, VD2*);

• amplifier-inverter (*VT1, VT2, VD3, R3, R4, R5*);

• element of connection diode logic to amplifier (*R2, VD3*). (*break down protection*)

The number of similar inputs determines the functionality of such elements and characterized by input combining coefficient (fan-out) K_{FO}. The fan-out coefficient is the number of inputs of a logic function that can be driven from a single output without causing any false output. It is a characteristic of the logic family to which the device belongs. For DTL, usually ≤ 8. *[K_{FO} =min(I_{out}/I_{in}) for high and low input signal]*

At the output of the logic circuit AND, an intermediate signal is formed $x' = x_1 \cdot x_2$, the level of which $U' = min\{U_{1i}\} + U_{od}$.

Through the *VD3* diode, this signal is received at the input of the inverter amplifier.

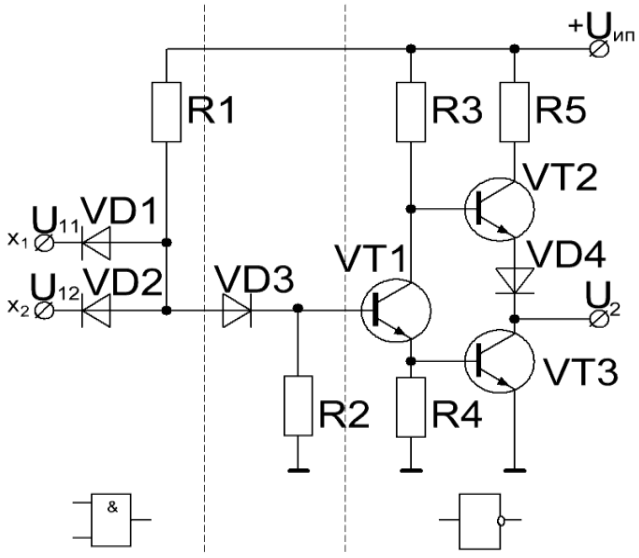


Fig. 2.1.

$$X' = X_1 \cdot X_2, \qquad U' = \min\{U_{11}, U_{12}\} + U_0.$$

The amplifier inverter contains 2 cascades:

The input phase-inverter cascade is constructed on a transistor *VT1*, which forms two anti-phase signals that control the operation modes of transistors *VT2* and *VT3*.

The output stage on transistors *VT2* and *VT3* provides switching of output between a general bus and a power supply.

The feature of this circuit is the use in the base circuit of the *VD3* transistor diode, which is designed to increase the threshold voltage of the transistor switch and prevent it from interfering with the input signals at the logical zero level. Resistor *R2* provides a return flow of collector junction in the mode of the cutoff of the transistor *VT1*.

To open the transistors *VT1, VT3,* it is necessary to lock the diodes *VD1, VD2* and open the *VD3* diode.

Therefore, the threshold voltage $U_{\text{пор}}$ is determined by:

$$U_{\text{пор}} = U_{0VD3} + U_{0VT1} + U_{0VT3} - U_{0VD1} \approx 1.4V,$$

where U_{0VD}, U_{0VT} are the threshold voltages of the corresponding diodes and transistors.

Let the input signal pass low level of input signal $U_1^0 < U_{\text{пор}}$. Under this condition, transistors *VT1, VT3* are locked, and *VT2* can be in any of the possible modes: depending on the method of connecting the load: the transistor can be locked if the load is connected to a power source, is in active mode or in saturation mode, if the load is connected between the output and the common bus.

If the load is connected to the "ground", then through the open transistor *VT2* can flow current, while at the output of the element set the high level of the output signal:

$$U_2^1 \cong U_{\text{ип}} - U_{0VD4} - U_{0VT3} - U_{R3}$$

At typical voltage of power $U_{\text{ип}} = 5\text{V}$ and $U_{0VD} = 0.7V$ (for silicon diodes).

$$U_2^1 = 5B - 0.7B - 0.7B = 3.4V$$

At a high level at the all inputs of the inverter, when $U^{'} > U_{пор}$, the transistor *VT1* goes into saturation mode. Through the resistors *R3* and *R4* current flows, due to the voltage drop on these resistors, the transistor *VT2* closes (goes into the cutoff mode), and the transistor *VT3* goes into saturation mode. At the same time the output is set to low signal level:

$$U' > U_{\text{пор}}, U_2^0 = I_{\text{н}}^0 . r_{\text{кнз}},$$

where $r_{кнз}$ is the resistance of the saturated transistor *VT3*.

Transmission characteristic of an element - the dependence of the output voltage on the dominant input signal is $U_1^*: U_2 = f(U_1)$. The type of transmission characteristics depends on the type and loading parameters (Fig. 2.2), where:

$$U_1 = min\{U_{1i}\}.$$

On the transfer characteristic, four distinctive areas can be distinguished.

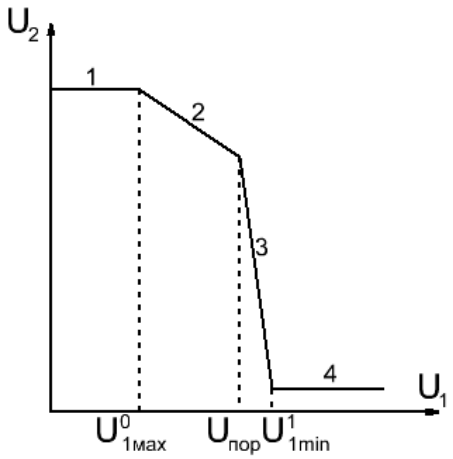


Fig. 2.2

In area 1, $U_1 < U_{\text{пор}}$ the transistors *VT1* and *VT3* remain locked, and at their output, the logic element is maintained constant voltage:

$$U_2^1 = U_{\text{ип}} - U_{\text{ОТ2}} - U_{0VD4}$$

In the region, 2 transistors *VT1* and *VT2* are in active mode, and the circuit has a voltage transfer coefficient:

$$K_{U_2} \cong -\frac{R_3}{R_4}$$

In this area, the noise immunity of a logical element deteriorates at the level of the logical zero. As it was mentioned, the threshold voltage increases due to the *VD3* diode.

$$U_{\text{пор}} = U_{0VT1} + U_{0VT3} + U_{0VD3} - U_{0VD1(2)}$$

If there was no *VD3* diode, the transistor *VT1* would open due to the slightest noise at the level of the logical "0", and the inclusion of the *VD3* diode necessitates the need for a resistor *R2*, and its resistance is selected from the condition:

$$R2.I_{k01max} \leq U_{01T1min},$$

where I_{k01max} is the maximum thermal current, $U_{0VT1min}$ is the minimum program voltage of the transistor *VT1*.

This follows from the condition of thermal stabilization. At the maximum temperature, the minimum voltage at the emitter junction *VT1* and the maximum thermal current $I_{ко1}$ are set.

In area 3, all transistors are in active mode, so the voltage transmission factor K_{U3} is maximal and the transmission characteristic is sharply decreasing.

In the region, 4 transistors *VT1* and *VT3* are saturated, the transistor *VT2* is locked and the output voltage of the logical zero is independent of the voltage U_1^*, but is determined by the load parameters:

$$U_2^0 = I_{\text{н}}^0 . r_{\text{кн3}},$$

where $I^0_{н}$ – current of external load. $r_{кн3}$ – resistance of transistor *VT3* in saturation mode.

2.2. Logic elements AND-OR-INVERT, NOR

In Fig. 2.3 is shown the example of the DTL, the element of the two-stage logic AND-OR-NOT. It consists a power amplifier circuit, which often used in integrated circuits on bipolar transistors.

Intermediate logic signals are defined by logical expressions:

$$X' = X_1 \cdot X_2,$$

$$X'' = X_3 \cdot X_4,$$

$$X^* = X' + X''.$$

Output: $Y = \overline{X^*} = \overline{X_1X_2 + X_3X_4}$ implements a two-step logical function.

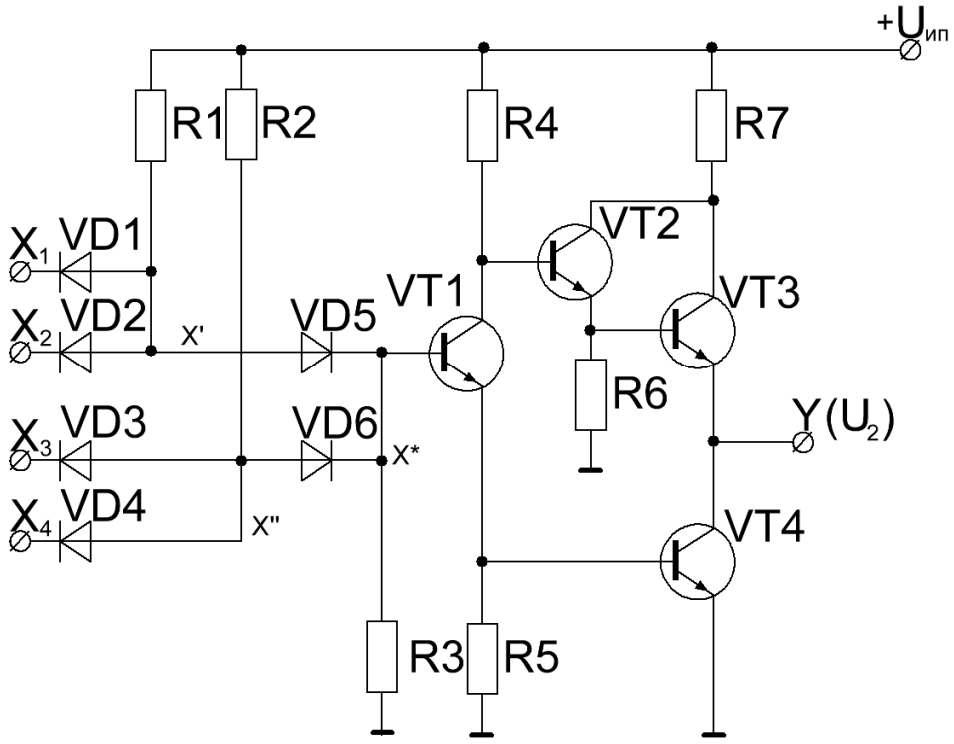


Fig. 2.3

Here, the first stage *VT1* has two phase-inverter outputs, which control the modes of the output cascade transistors on the composite transistor *VT2*, *VT3* and the transistor *VT4*. The resistor *R6* provides the drainage of the thermal current necessary to ensure the temperature stability of the transistor *VT3*. If the input signal is:

$$U_1 = max\{min(U_{11}, U_{12}), min(U_{13}, U_{14})\} = max\{U_1', U_1''\} < U_{\text{пор}}^0$$

then transistors *VT1* and *VT4* are locked, and *VT2* and *VT3* are open and the output is formed by a high level:

$$U_2^1 = U_{\text{ип}} - I_{\text{к}01}R3 - U_{OT2} - U_{OT3},$$

where U_{OT2}, U_{OT3} - the voltage drop across emitter transistor transitions correspondently to *VT2* and *VT3*.

If transistors *VT1*and *VT4* are saturated, and *VT2*, *VT3* are in the cutoff mode. The output level is set to low:

$$U_2^0 = I_{\text{н}}^0 i_2 r_{\text{кн.}}.$$

In both states, the through current through transistors *VT2*, *VT3* and *VT4* does not leak, since in this circuit always one transistor is locked. Due to this, the output resistance of the DTL-element in both logical states is small. The through current through the output cascade can proceed in the transitive mode from the logical zero to the logical unit at the output. For its limitation, a resistor *R5* is included in the circuit. The ability to load such elements reaches $K_{роз} = 10$ and above.

The separate case of the scheme, which is presented in Fig. 2.3, is when the input circuits AND have only one input:

$$X' = X_1,$$

$$X'' = X_3.$$

That responds to the implementation of the logical element NOR:

$$Y = \overline{X_1 + X_3}.$$

3. Transistor - transistor logic (TTL)

Transistor-transistor logic (TTL) elements are the technological development of DTL elements and are still in use. The simplest TTL element can be obtained from the DTL element by replacing the group of input diodes *VD1*, as well as the displacement diode *VD3* by a multi-emitter bipolar transistor (MET) with the number of emitters corresponding to the number of inputs m (Fig. 3.1).

Transmission characteristic of this scheme is similar to the characterization of the DTL element. The difference is to change the threshold voltage:

$$U_{\text{пор}} \approx U_{\text{К}H1} + U_{0VT1} + U_{0VT4},$$

where $U_{\text{К}.H1}$ - the voltage of the collector-emitter of saturated MET; U_{0VT1}, U_{0VT4} - threshold voltage of transistors *VT1*, *VT2*. Input current I^1 at a high level of the input signal U_1^1 is greater than in the DTL element, because it is the current of the transistor *VT1* in the inverse active mode.

3.1. The basic element of the NAND (Sheffer-element)

The scheme of the basic TTL element of classic series, implementing the logical function of NAND, is shown in Fig. 3.1.

In the system of positive logic, the transistor MET with the resistor *R1* in the base chain implements the logical operation "AND", and the push-pull power amplifier based on transistors *VT1*, *VT2*, *VT4* (*VT3* is used as a diode), performs the function NOT, provides the formation of standard logic levels of the output signal and the coordination of the TTL-element with a given load.

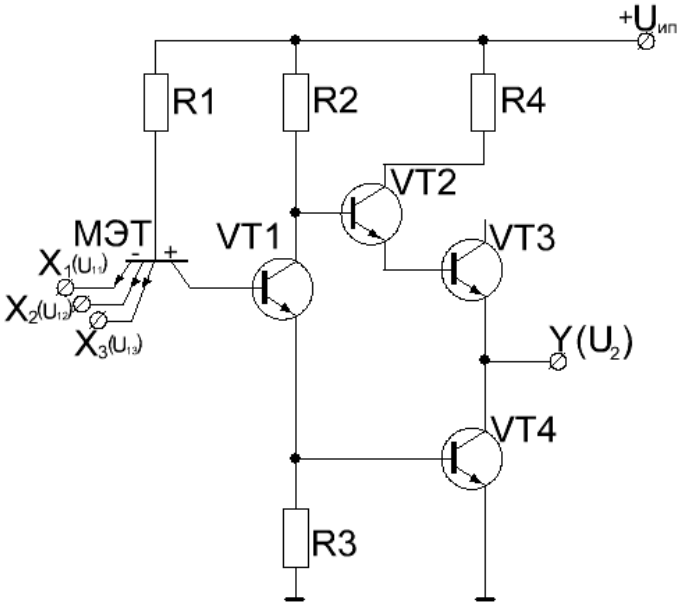


Fig.3.1

The mode of operation of MET and input current is determined by the dominant input signal:

$$U_1^* = min\{U_{1i}\}, i = \overline{1,m},$$

as well as the input impedance of the transistor *VT1*. If the potential of the base of the transistor *VT1* $U_{Б1}$is less than the threshold voltage U_{01} (for silicon transistors $U_0^{Si} \approx 0.7B$), the transistor *VT1* is in the cutoff mode and its collector maintains high potential $U_{k1} \approx U_{u.n}$ and the emitter is low $U_{E1} = U_{Б4} \approx 0$. Therefore, the transistor *VT4* is also locked, and the transistors *VT2*, *VT3* are open (in active mode). When the load is depleted, current through *VT2*, *VT3* is determined by the reverse current of the collector transition of the transistor *VT4* $I_{К.0}$. Input impedance of the transistor *VT1* is large (resistance to the leakage of its collector junction) and the input current is small: $I_{Б1} = -I_{К.01}$. With the increase in the potential $U_{Б1} > U_{01}$, the transistor *VT1* goes into active mode, the currents $I_{К1}$ and I_1increase and the potential U_{E1} increases and the collector $U_{К1}$ voltage decreases. While the potential $U_{Е1}$ is not sufficient to open the transistor *VT1*, the input impedance of the transistor *VT1*

$$R_{вх1} = r_{Б1} + (\beta_1 + 1)(\phi_Т / I_{Б1} + R3) \approx R3\beta_1[\phi_T/(U_{Б1} - U_{01}) + 1],$$

the input current remains large $I_{Б1} = I_К$ slightly increasing. At the moment of opening the transistor *VT4* is full emitter resistance $R_{вх4} = [r_{б4} + (\beta_4 + 1)\phi_T / I_{Е4}]||R_3$ and, consequently, the input impedance of the transistor *VT1* sharply decreases and correspondingly increases the current $I_{б1}$.

Thus, the input impedes sharply at $U_{Б1} \approx U_{01} + U_{04} = U_{пор} \approx 1{,}4В$. Therefore, for any combination of input signals, if $U_1^* < U_{пор}$, MET base current

$$I_Б^0 = (U_{И.П.} - U_1^* - U_0)/R1$$

flows through one or more MET straightforward emitter transitions and supports it in saturation mode. Since the voltage collector is an open emitter in the saturation mode of the transistor $U_{К.Н.} \approx 0$, we can assume that $U_{Б1} = U_1^* + U_{К.Н.} \approx U_1^*$, that is the input voltage of the amplifier $U_{Б1}$ is equal to the smallest of the input voltages.

If $U_1^* > U_{пор}$, all MET emitters are displaced in the opposite direction, while the collector is in the forward direction and MET operates in the inverse active mode.

On the collector of the saturated transistor *VT1* and the base *VT2* there is a low potential consisting of the voltage at the open emitter transition of the transistor *VT4* and the residual saturation voltage of the transistor *VT1*:

$$U_{К1}^0 = U_{Б2}^0 = U_{Б4} + U_{КН1} \approx U_{Б4}.$$

Output voltage U_2^0 is determined by the voltage of the collector-emitter transistor *VT4* in the saturated state and proportional to the load current I_2:

$$U_2^0 = r_{кн4} I_2,$$

where $r_{КН4}$ - resistance between the collector-emitter of the saturated transistor *VT4*.

In the case of saturation of the transistor *VT1* between the base of the transistor *VT2* and the emitter of the transistor *VT3*, taking into account the two previous formulas, the voltage $U_{Б2-Е3} = U_{Б2} - U_2^0 = U_{Б4} + U_{КН1} - r_{КН4} I_2$.

In the worst case at idle on the way out $I_2 = 0$ high-voltage $U_{Б2-Е3}$ is maximum $U_{Б2-Е3} \approx U_{Б4} \approx 0{,}7V$. This voltage is capable of opening one emitter junction, but it is not enough to unlock two consecutive transitions of the transistors *VT2* and *VT3*. Therefore, an output transistor *VT3* in the diode mode is introduced in the output circuit, which ensures the guaranteed locking of the transistor *VT2*, when *VT1* is in saturation mode.

3.2. Modifications of LE NAND

3.2.1. LE with free collector

Sometimes there is a need to use for controlling the load of logic element (LE), which have a separate power sources with high consumption current. Such a load can be a relay winding, a light indicator, etc. For this purpose, LE is used, in the collector circuit of the output transistor, which there is no resistor, and therefore it is called a logical element with a free collector. Simplified scheme of such LE is shown in Fig. 3.2, where $R_н$ - external load of the chip. For this case:

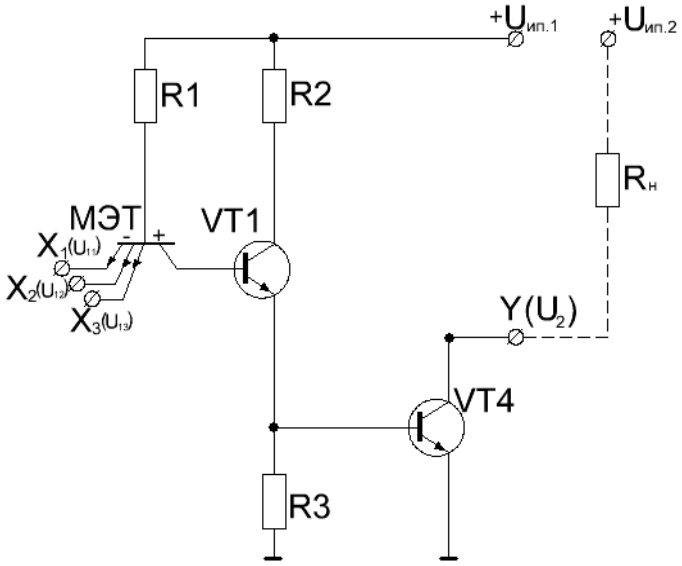


Fig. 3.2

$$U_2^1 = U_{\text{ип2}} - I_{\text{ко4}} \cdot R_{\text{н}} \approx U_{\text{ип2}}$$

$$U_2^0 = I_{\text{кн4}} \cdot r_{\text{кн4}} = \frac{U_{\text{ип2}}}{R_{\text{н}} + r_{\text{кн4}}} \cdot r_{\text{кн4}}$$

For normal operation, the collector of the output transistor *VT4* should be connected, as shown in Fig. 3.2, to the power supply through the external load circuit. In this case, the external devices that connect to the output, can operate from other sources of power ($U_{\text{ип2}}$) with higher voltage.

LE with a free collector allows the parallel connection of several LE's to the total load (Fig.3.3). With such a connection, if the on output of one of the elements is low potential U_2^0, then the output of the entire system will also have a logical zero. To provide a high level of potential U_2^1 at the common output, it is necessary to close the output transistors of all LE's, i.e. to set them in the state of the logical unit. Thus, by creating a system that performs the "AND" operation, a parallel connection of

several open collectors with a total load can be created. In Fig. 3.3 gives an example of an assembly of two chips. In this case:

X'	X''	Y
0	0	0
0	1	0
1	0	0
1	1	1

$$X' = \overline{x_1 x_2 x_3};\ X'' = \overline{x_4 x_5}$$

$$Y = X' \cdot X'' = \overline{x_1 x_2 x_3} \cdot \overline{x_4 x_5} = \overline{x_1 x_2 x_3 + x_4 x_5}$$

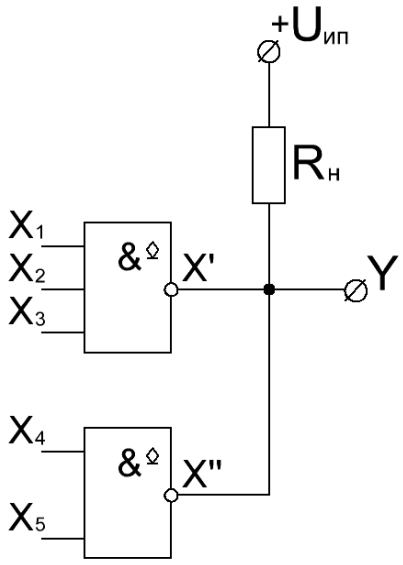


Fig 3.3

Such a connection with an open collector is called "assembling AND".

3.2.2. LE with block

In Fig. 3.4 shows an LE with an input V, which provides, when V = 0, to disconnect the output of the chip from the load:

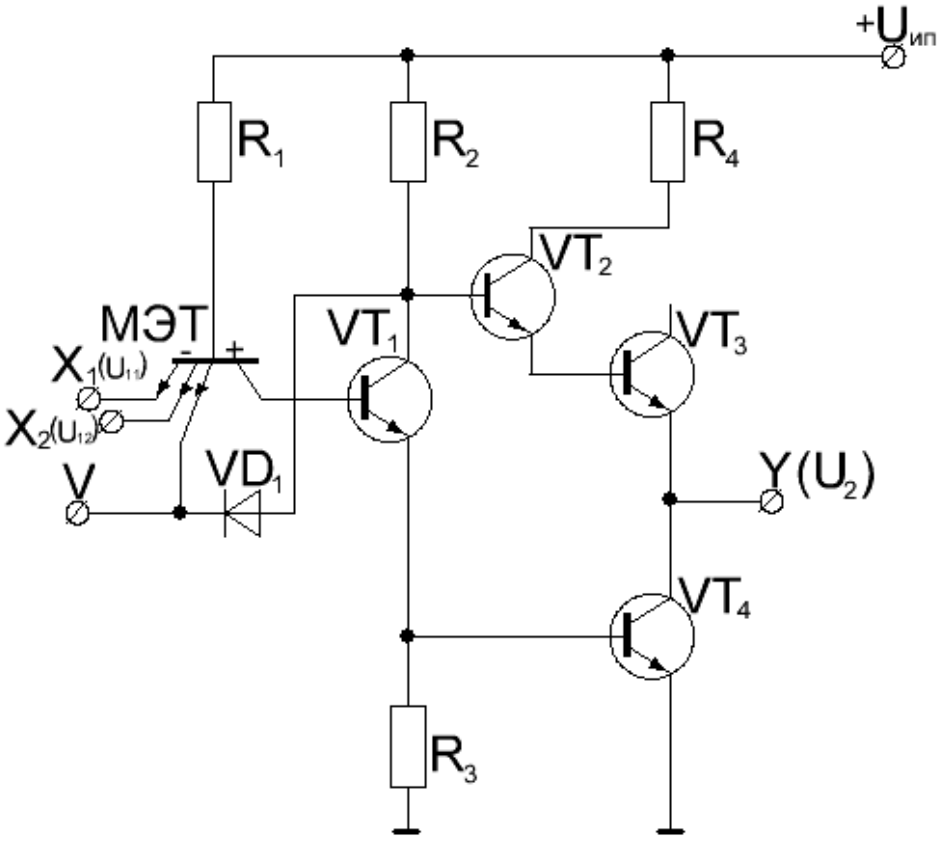


Fig. 3.4

If input V is applied 1: V = 1, then. $Y = \overline{X_1 X_2}$.

At V = 0 the output is disconnected, the transistors *VT2* and *VT4* are closed. This is a state of high-resistance output. In this case, the state of output *Y* is determined by the external circuit.

Block inputs enable the inclusion of TTL elements on the common signaling bus.

3.3. LE AND-OR-NOT, NOR

The basic ICs of the TTL series include elements that implement the AND-OR-NOT, NOR logic functions.

In Fig 3.5 shown the circuit of the logic element 2-2AND-2OR-NOT.

Logical variables in the scheme are determined by the relationships:

$X' = X_1X_2$, $X'' = X_3X_4$, $Y' = X' + X''$, $Y = \overline{Y'} = \overline{X' + X''} = \overline{X_1X_2 + X_3X_4}$.

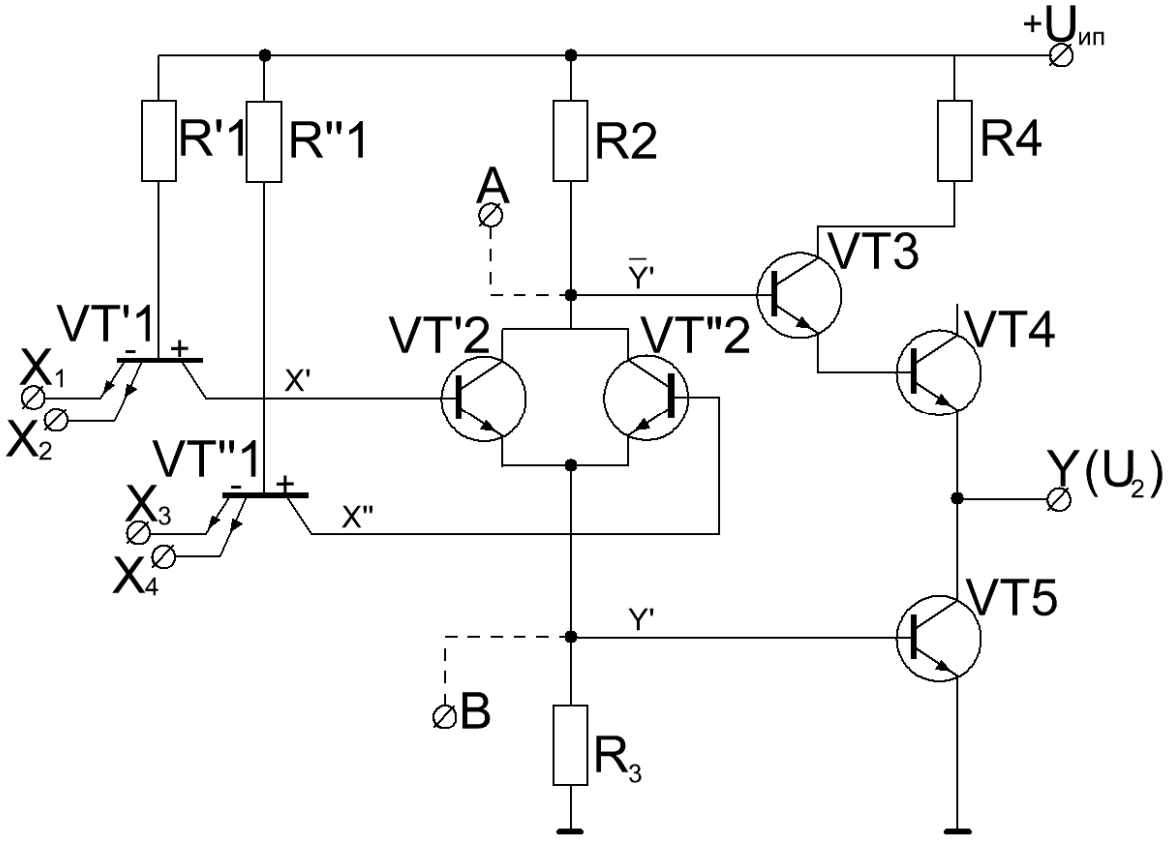


Fig. 3.5

Here the logic function AND is realized by multi-emitter transistors *VT1'* and *VT1"*, similar to the scheme NAND. The function OR is implemented by the parallel including transistors *VT2'* and *VT2"*. If at least one of them is open, through the resistors *R2, R3* flows the current, which creates for the transistor *VT3* locking, and for the *VT5* - opening potentials on the base and on the output of the element is set to a logical zero. If *VT2'* and *VT2"* are locked at the same time, the output level is set to U_2^1. The number of inputs for AND may be different for each of the groups, but usually $K_{ass.\text{AND}} \leq 8$. In a specific case, when each of the transistors *VT1'* and *VT1"* has one emitter, we obtain an element of one-stage NOR-logic. The number of inputs (groups) for AND is limited ($K_{ass.\text{OR}} \leq 4$) by considerations of speed and temperature stability, as well as the parallel inclusion of the transistors *VT2'* and *VT2"* increases the equivalent capacity of the load of the phase-inverter cascade, while through the resistor *R2* flows the total thermal current I_{K0} of the transistors *VT2*.

In Fig. 3.5 shown the outputs A, B, which can be used to connect additional external circuits that extend the logic capabilities of an element using a logic extender

(Fig 3.6-a). In the circuit, shown in Fig. 3.6, the output signal is determined by the expression:

$$Y = \overline{X_1X_2 + X_3X_4 + X_5X_6X_7}.$$

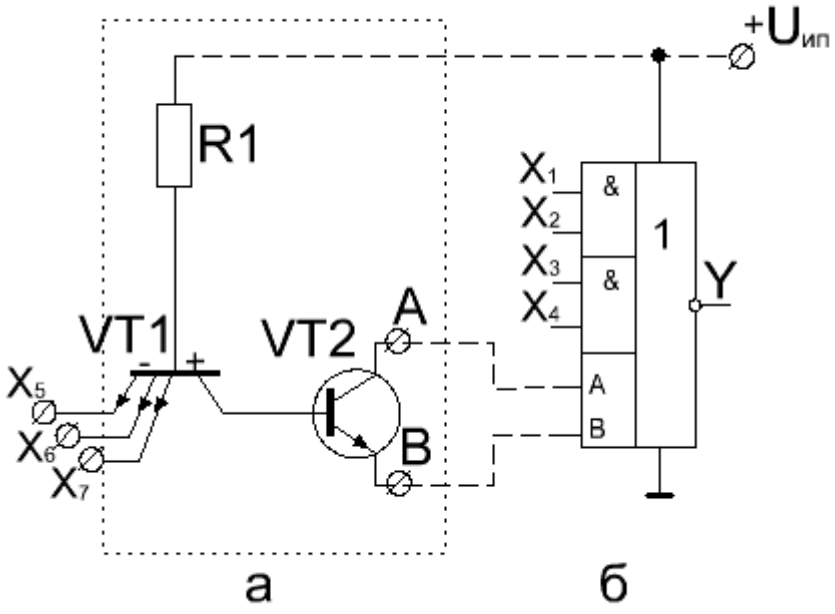


Fig. 3.6

4. Emitter- coupled logic (ECL)

The digital elements of emitter-coupled logic (ECL) are based on current switches and differ from other types of IC's with the highest speed, but also with high power consumption. High speed (or low switching cycle time) in ECL elements is due to the fact that bipolar transistors in these circuits operate without saturation, that is, they can be either in active mode or in cut-off mode. Another important factor for increasing the speed is the use of low-resistance resistors in the elements that provide a quick recharge of parasitic capacities by increasing the power consumption and reducing the difference in logic signals, and thus the impedance of ECL elements. A circuit's tool for increasing the speed is the use of emitter repeaters that provide reloading of capacities in the load chains through small output supports. At the same time, the load capacity increases: $К_{роз} \leq 15$.

Fig 4.1 shows the circuits of the basic logic element of the ECL, which implements the logic function 2NOR.

Structurally, such a circus is a bridge, to one of the diagonals that fed through the source U_{un} of a stable current I_0. From the other diagonal (collectors of transistors *VT1* and *VT2*), the output signal is removed. The base of the transistor *VT2* provides constant potential $U_{оп}$ (reference voltage) from the source of the reference voltage. If

R_1=R_2=R_k and to the base of the transistor *VT1* come the potential $U_1 = U_{оп} < I_0 R_к$, then when the parameters of the bridge transistors coincide, it is balanced $i_{к1} = i_{к2} = 0.5I_0$ і $U_{21} = U_{22} = 0.5R_к I_0$. In this case, both transistors are in active mode and there is a transistor-amplifying cascade with an emitter connection and a symmetric (phase-inverse) output. In digital circuitry, this cascade is used in switching mode. For this, the reference voltage is chosen from the ratio of logical levels (U_1^0, U_1^1) control signal: $U_{оп} \approx 0.5(U_1^0 + U_1^1)$.

4.1 Basic logic element OR / NOR

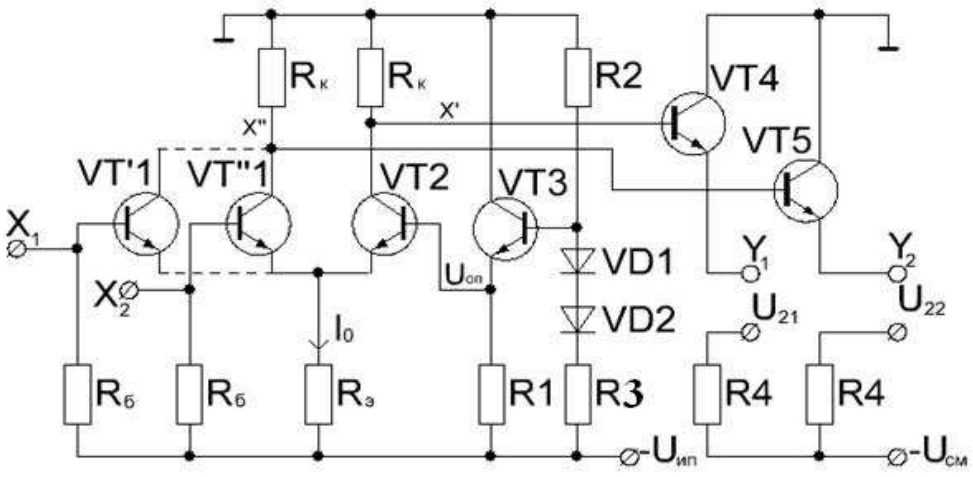


Fig. 4.1

Construct a truth table for the two input signals and see how the transistors behave for each of the combinations. Logic of the circuit:

X_1	X_2	Y_1	Y_2
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

$$X' = X_1 + X_2$$

$$X'' = \overline{X'} = \overline{X_1 + X_2}$$

$$Y_1 = X' = X_1 + X_2$$

$$Y_2 = X'' = \overline{X_1 + X_2}$$

In the circuit in Fig. 4.1, the current switch is constructed on a transistor *VT2* and a group of parallel-transmitted transistors *VT1* according to the number of logical inputs of an ECL element. The total emitter current of transistors *VT1* and *VT2* is stabilized by high-resistor $R_э$. The reference voltage $U_{оп}$is determined by the resistive divider *R2*, *R3* voltage, which through the emitter repeater made on the transistor *VT3*, is fed to the base of the transistor *VT2*. For the temperature compensation of the voltage in the base circuit of the transistor *VT3* included diodes *VD1*, *VD2*. Emitter repeaters on the outputs of the ECL element (transistors *VT4* and *VT5*) provide amplification of the output signal by current and power, as well as the harmonization of the levels of input and output signals, reducing the signal levels at the outputs of the ECL element to $U_0 \approx 0.7V$ (lower than the potentials of the collectors of transistors *VT1* and *VT2*). An external jumper connects emitter resistor *R4* if necessary. This makes it possible to combine the outputs of several ECL elements into the "assembling OR" on one common resistor *R4* (Fig. 4.2).

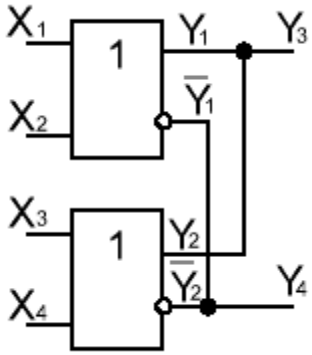


Fig. 4.2

$$Y_3 = Y_1 + Y_2 = X_1 + X_2 + X_3 + X_4$$

$$Y_4 = \overline{Y_1} + \overline{Y_2} = \overline{X_1 + X_2} + \overline{X_3 + X_4} = \overline{(X_1 + X_2) \cdot (X_3 + X_4)}$$

Resistors $R_Б$ designed to securely lock transistors *VT1* on unused inputs. To improve the noise immunity of an element, usually the "ground" bus is divided so that the internal logical elements are connected to one bus, and the emitter repeaters to the other. In this case, impulse interference in powerful circuits of emitter repeaters does not affect the operation mode of the switch of current.

Let us consider in more detail the principle of the basic ECL element (Fig. 4.1), which is based on the operation of the switch on the transistors *VT1* and *VT2*. The potential of the general emitter of the transistors *VT1* and *VT2* depends on the voltage of the dominant *m* input signals U_{1i}:

$$U_1^* = max\{U_{1i}\},\ i = \overline{1, m}.$$

The potential of the transistor base *VT3* is determined by the divider: $U_{Б3} = \frac{U_{ип}-2U_0}{R2+R3} \cdot R2$, and reference voltage: $U_{оп} = U_{Б3} - U_{О3} = const = U_{Б2} = -1.3V$.

Then the current: $I_0 = \frac{U_{оп}-U_0}{R_э} = const$.

Voltage levels on collectors *VT1* і *VT2* while $U_1^* = U^0$:

$$U_{К1}^1 = -I_{КО} \cdot R_К \cdot К_{ОБ} \approx 0V$$

where $К_{ОБ}$ – the blockage factor at the input (number of inputs);

$$U_{К2}^0 = -I_0 \cdot \alpha \cdot R_К \approx -0.9V.$$

As already mentioned, the transistors *VT4* and *VT5* in addition to the current gain provide the conform of input levels, reducing the potentials of collectors VT1 and *VT2* by the value U_0:

$$U_{21} = U_{K2} - U_{04}, \text{ i.e. } U_2^0 = -0.9 - 0.7 \approx -1.6V,$$

$$U_{22} = U_{K1} - U_{05}, \text{ i.e. } U_2^1 = 0 - 0.7 = -0.7V$$

Thus, the feature of these elements is:

- high speed;
- relatively high power consumption;
- small difference of voltage levels (U_2^0 = -1.6V; U_2^1 = -0.7V);
- no binding of logic levels to supply voltages.

4.2 Basic logic element E²CL

In the logical elements of E²CL the last drawback is eliminated (Fig. 4.3).

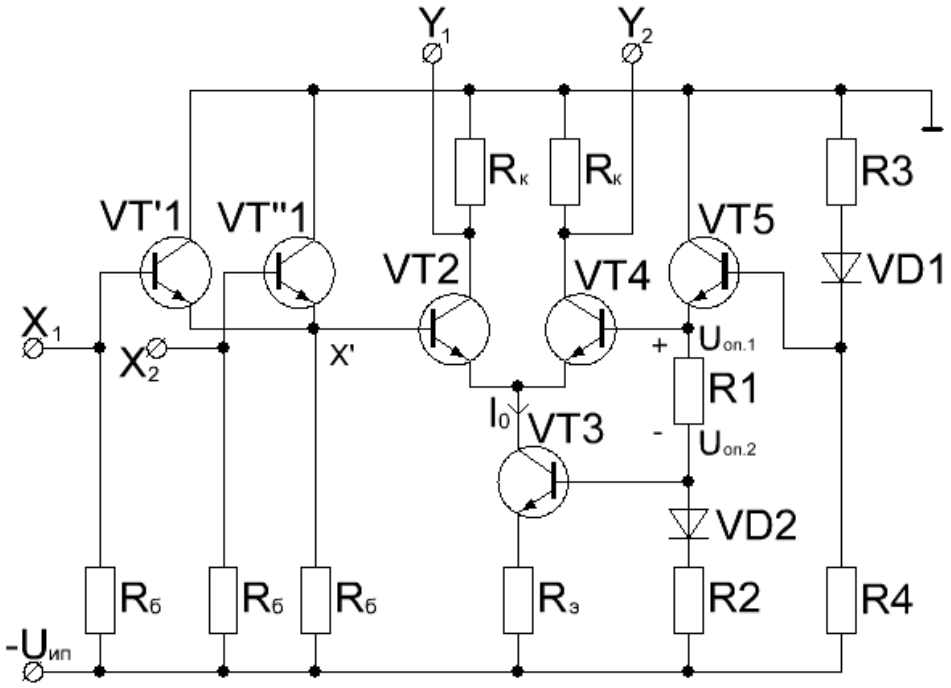


Fig. 4.3

The logic of the element is similar:

$$X' = X_1 + X_2$$

$$Y_1 = \overline{X'} = \overline{X_1 + X_2}$$

$$Y_2 = \overline{Y_1} = X' = X_1 + X_2$$

In this circuit, the transistor *VT3* is a stable current generator I_0.

$$U_{\text{оп.1}} = \frac{-U_{\text{ип}} - U_{0VD1}}{R3 + R4} \cdot R3 - U_{0VT5}$$

$$U_{\text{оп.2}} = -\frac{U_{\text{оп.1}} - U_{\text{ип}} - U_{0VD2}}{R1 + R2} \cdot R1 + U_{\text{оп.1}}$$

$$I_0 = \alpha \cdot I_{Э4} = \frac{U_{\text{оп2}} - U_{0VT4} - U_{\text{ип}}}{R_Э} = const$$

$$U_2^0 = -I_0 \cdot R_K \approx -0.9V$$

$$U_2^1 = -I_{K0} \cdot R_K \approx 0V$$

Transistors *VT1*' and *VT1*" perform the function of conforming the levels of input and output potentials and increase the input impedance.

The *VD2* diode provides thermal stabilization of the current I_0, and *VD1* is the thermostabilization of the threshold level of the switching signals.

In the circuits E^2CL - elements (Fig. 4.3) the matching of the signal levels is transferred from the outputs to the input, which is the *m*-input emitter repeater. Speed of the E^2CL-element is higher, since the equivalent input capacities of the cascade with the common collector are lower than the cascade with the total emitter, the equivalent capacity of the collector of the inverting transistor *VT2* is also less and does not depend on the number of inputs. Output resistance E^2CL-element $R_{\text{вых}} = R_K$ higher than that of ECL elements, but the branching factor $K_{\text{раз}}$ does not decrease because of the large supports of the input load cells. The high level of the logic signal is practically equal to the potential of the earth, which reduces the effect of interference and facilitates the connection with logical elements such as DTL and TTL.

5. Logic elements on MOS transistors

Properties, electrical parameters and characteristics of logic elements on MOS - metal–oxide–semiconductor transistor are completely determined by the properties of electronic switches on which such elements are constructed.

5.1. LE NAND type

The basic NAND element is based on successively included MOS transistors, the number of which is determined by the required number of inputs *m* with the general linear or nonlinear loads, as well as on the basis of *m* complement pairs.

5.1.1. n-MOS technology

Let we implement the basic function of algebra of logic (Fig. 5.1) $= \overline{X_1 \cdot X_2}$.

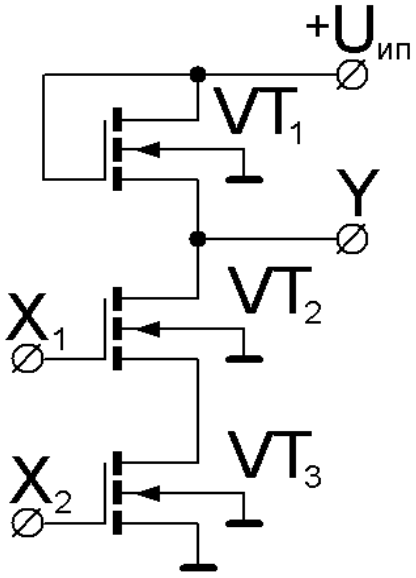


Fig 5.1

The NAND logical element is constructed using two transistor switches VT_2 and VT_3, which connect consistently with the total load VT_1 (Fig. 5.1). In this circuit, both switches will be closed, creating a path for current and providing a low output voltage U_2^0 only at $X_1 = X_2 = 1$. If one of the inputs to provide a logical zero, for example, $X_2 = 0$, then the transistor VT_3 will close, the current in the serial circuit of the transistors is absent and the output will be high voltage U_2^1. Thus, the output signal Y will be obtained according to the truth table:

X_1	X_2	Y
0	0	1
0	1	1
1	0	1
1	1	0

That is: $Y = \overline{X_1 \cdot X_2}$.

Here, $X = 0$ means that the input signal $U_1^0 < U_{\text{пор}}$. At the same time, $Y = 1$, which corresponds to the output potential. $U_2^1 = U_{\text{ип}} - U_{\text{пор1}}$.

If $X_1 = X_2 = 1$, then the output LE is set to $Y = 0$, which corresponds, for

$$U_2^0 = (U_{\text{им}} - U_{\text{порз}}) \cdot \frac{K_{\text{об}} \cdot R_i}{R_{i\text{з}} + R_i \cdot K_{\text{об}}} \to 0, \text{ if } R_{i\text{з}} >> R_i \cdot K_{\text{об.}},$$

where R_i - differential resistance of the corresponding transistors.

Association coefficient $K_{об}$, is not high, especially in the elements NAND ($K_{\text{об}} \leq 4$), since with the increase in the number of inputs $K_{об}$, the level of the logical "0" grows:

$$U_2^0 = \frac{U_{\text{им}} - U_{\text{пор}}}{R_{\text{iн}} + K_{\text{об}} \cdot R_{\text{i}}} \cdot K_{\text{об}} \cdot R_{\text{i}},$$

where $R_{ін}$ - resistance of the transistor-load (in Fig. 5.1 is VT_1).

In addition, with the growth of $K_{об}$, the duration of the front $t_{\text{ф}}^{10}$ of the output signal increases:

$$t_{\text{ф}}^{10} = 3 \cdot \text{C}_{\text{н}} \cdot R_i \cdot K_{\text{об}},$$

Loading capacity of MOS-elements of all types is large (up to 20), because the output current in them is small. This is due to the very large input impedance that loads the output of the MOS transistors (over than 10^{12} Ω). However, it should be borne in mind that the increase in the number of load cells, as well as the increase in parallel connected input transistors, leads to an increase in loading capacities and, as a consequence, to decrease the speed.

5.1.2. CMOS technology

The NAND logical element is implemented by means of two CMOS (complementary metal–oxide–semiconductor) switches by parallel switching of p-channel transistors and serial connection of n-channel transistors. Fig. 5.2 shows the electrical circuit of the two-input element, NAND.

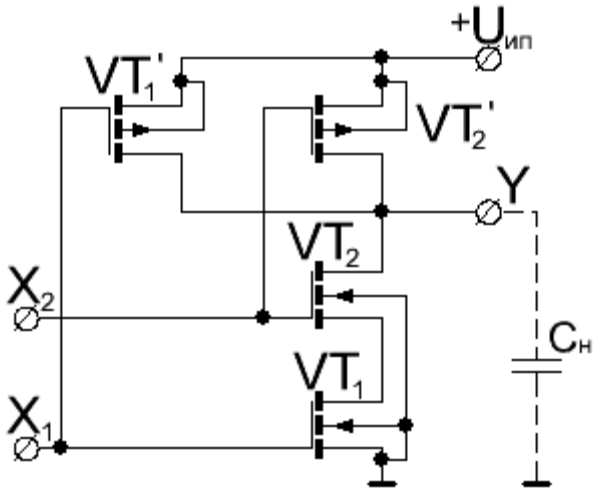


Fig.5.2

If both input voltage are high, the transistors VT_1 and VT_2 are open, and VT_1' and VT_2' are locked. The output voltage is close to zero, $U_2^0 \approx 0$, i.e Y=0.

If at least one of the inputs has a logical zero, for example $X_1=0$, then the transistor VT_1 is locked, and the transistor VT_1' is opened and therefore $U_2^1 = U_{\text{ип}}$.

For all cases, the current consumption $I_{\text{потр}}^{1,0} = 0$.

Duration of the output signal fronts:

$$t_{\text{ф}}^{01} = 3\tau^{01} = 3C_{\text{н}} \cdot R_{ip},$$

$$t_{\text{ф}}^{10} = 3\tau^{10} = 3C_{\text{н}} \cdot R_{in} \cdot K_{\text{об}} > t_{\text{ф}}^{01},$$

where R_{ip}, R_{in} — differential resistance of an open p- and n-channel transistor respectively;

$C_н$ – equivalent capacity load.

The main advantage of the CMOS-elements is that in both of their static states, the current from the power source does not almost flow, so the power consumed is very small. However, during operation of an element, the current charges unwanted capacitances, so the dynamic power consumption is proportional to the switching frequency and can be several stags higher than the static one.

5.2. LE NOR type

In logic elements NOR electronic switches are combined into a parallel group of inputs: $m \leq K_{об}$. Resistance of group of multipled transistors is determined by the least from parallel links, i.e. by a transistor on the breech-block of that the most is given from entrance voltages.

5.2.1. n-MOS-technology

Fig. 5.3 shows the circuit that implements the function $Y = \overline{X_1 + X_2}$:

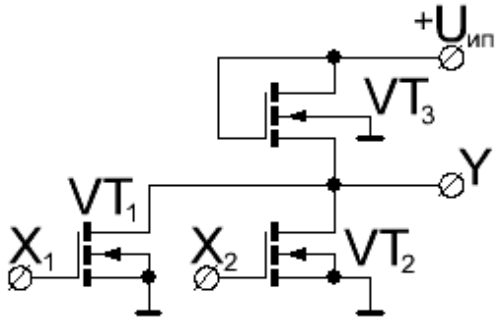


Fig. 5.3

If both inputs have a low logic zero ($X_1 = X_2 = 0$) level, transistors *VT1* and *VT2* are locked and the output will have a high voltage level: *Y = 1*.

If to apply a high level of the logical unit to at least one of the inputs, for example, the VT_2 transistor opens, that is output *Y* through a small resistance R_i will be connected to the common bus and the output voltage will be low, that is *Y = 0*. Thus, the output signal *Y* is determined by the table states:

X_1	X_2	***Y***
0	**0**	**1**
1	**0**	**0**
0	**1**	**0**
1	**1**	**0**

The logical "unit" at the output ($Y = 1$) responds to the voltage. $U_2^1 = U_{\text{ип}} - U_{\text{пор.з}}$.

Logical "zero" at the output ($Y = 0$) responds to the voltage. $U_2^0 = \frac{U_S - U_{\text{пор.з}}}{R_{i2} + R_i} \cdot R_i = I_{\text{пот}}^0 \cdot R_i$.

These elements have a drawback - they consume current ($I_{\text{пот}}^0$) with all combinations of input signals except one: $X_1 = X_2 = 0$.

5.2.2. CMOS-technology

The NOR logical element is realized by parallel switching of n-channel transistors and serial connection of p-channel transistors. Fig 5.4 shows the electrical circuit of two-input element NOR with elements of protection of inputs from static interferences.

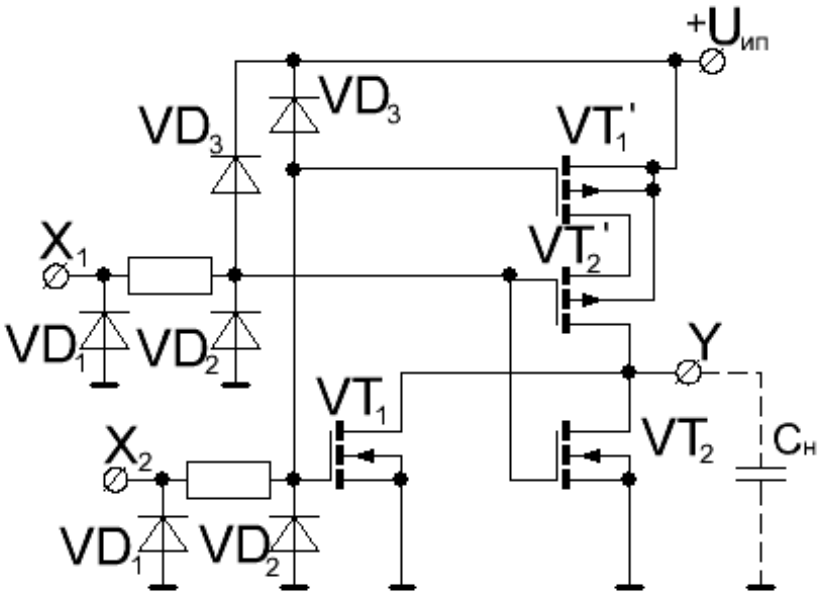


Fig 5.4

If on entrances it is given voltages of low levels, $X_1 = X_2 = 0$, then the transistors VT_1 and VT_2 are locked, and the transistors VT_1' and VT_2' are opened. The current in the power circuit is very small. The voltage at the output is close to the supply voltage: $U_2^1 = U_{\text{ип}}$, i.e. $Y = 1$.

If at least one, of the inputs is a logical unit, for example X_1=1, then the transistor VT_1 opens, and the transistor VT_1' closes. The current in the power circuit will still be small, and the output voltage, that is, $U_2^0 \approx 0$, $Y = 0$.

Diodes and resistors at each input provide protection of inputs from the static voltage on the external outputs of the chassis.

Diodes *VD₁* and *VD₂* protect inputs from negative pulsation at the logical zero level ($U_1^0 \ll 0$), and *VD₃* diodes - from positive pulsation at the level of the logical unit ($U_1^1 \gg U_{\text{ип}}$).

The current in the static mode is zero for all cases. $I_{\text{потр}}^{10} = 0$. The duration of the front of the output signal

$$t_{\text{ф}}^{01} = 3\tau^{01} = 3\text{C}_{\text{н}} \cdot R_{ip} \cdot K_{\text{об}} ,$$

$$t_{\text{ф}}^{10} = 3\tau^{10} = 3\text{C}_{\text{н}} \cdot R_{in},\ t_{\text{ф}}^{10} < t_{\text{ф}}^{01}.$$

For internal logic elements of any microcircuit, protection against static electricity is not provided (Fig. 5.5).

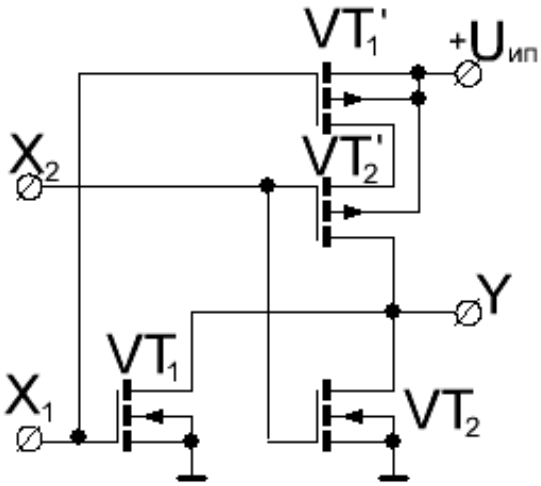


Fig. 5.5

5.3. Elements of two-level logic

The logical elements of the two-stage logic are constructed in the form of combinations of successive and parallel groups of MOS-transistors.

5.3.1. n-MOS technology

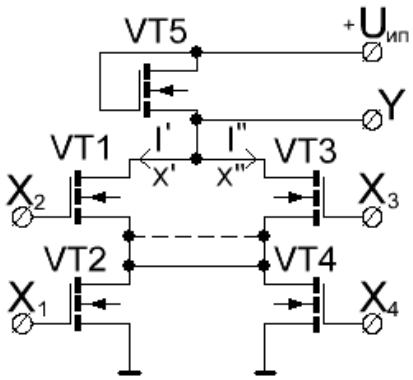


Fig. 5.6

If there is no jumper between *VT2* and *VT4* (dotted) in the circuit (Fig. 5.6), each of the pairs of sequentially connected transistors *VT1*, *VT2* and *VT3*, *VT4* in the positive logic system implements a logical multiplication operation and currents (X ', X ") flow , if $X_1X_2 = 1$ (or $X_3X_4 = 1$). If any of the *X'*, *X"* currents or their sum pass through the load transistor *VT5*, the low potential is set at the output, that is, the logical element implements the function AND-OR-NOT. The table of output states has the form:

X'	X''	**Y**
0	0	**1**
0	1	**0**
1	0	**0**
1	1	**0**

Then in the absence of a jumper: $X' = X_1 \cdot X_2$, $X'' = X_3 \cdot X_4$ and the output function looks like:

$$Y = \overline{X' + X''} = \overline{X_1X_2 + X_3X_4}.$$

A logical element over, that will realize this function, is shown on in Fig. 5.7-*a*.

In the presence of jumpers, the output function changes:

$$Y = \overline{(X_1 + X_4) \cdot (X_2 + X_3)}.$$

Graphic representation of such an element is shown in Fig 5.7-*б*.

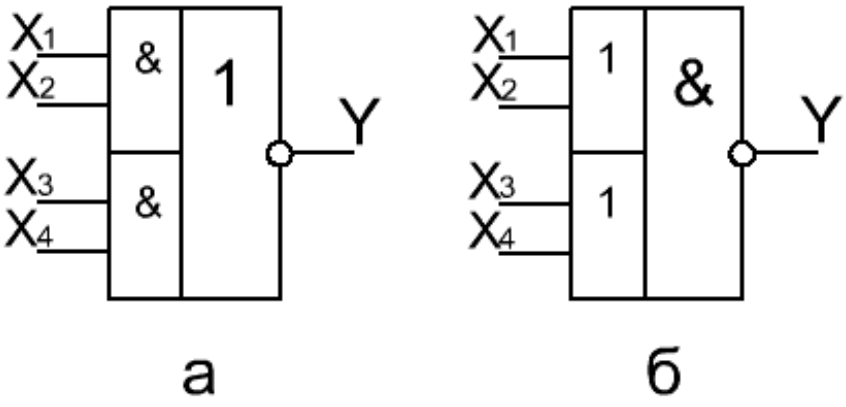


Fig. 5.7

5.3.2. CMOS-technology

In the digital circuitry, logical elements that implement the operation of the arithmetic addition of two variables are widely used. To do this, must be calculated a function $Y = X_1\overline{X_0} + \overline{X_1}X_0$, that can be implemented on the CMOS-transistors:

$$Y = X_1\overline{X_0} + \overline{X_1}X_0 = X_1 \oplus X_0 = \overline{X_1 \sim X_0}.$$

The circuit that implements the function EXCLUSIVE OR on the CMOS-transistors is shown in Fig. 5.8.

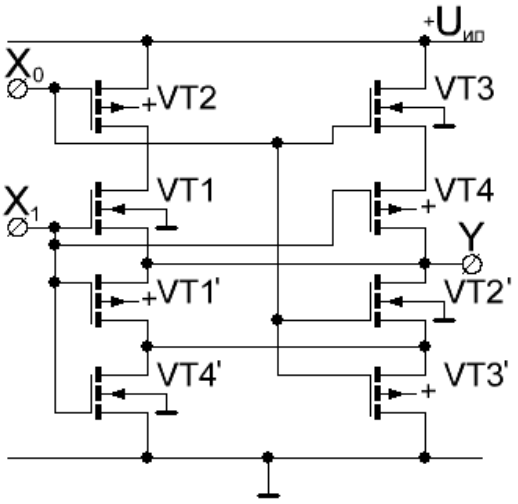


Fig. 5.8

X_1	X_0	Y
0	**0**	**0**
0	**1**	**1**
1	**0**	**1**
1	**1**	**0**

General rule for construction of two-stage logic on CMOS-transistors:

To build a two-level logic on the CMOS you need:

• bring the function to the form of MDNF or MCNF;

• for each intermediate module (MDNF), the serial circuit of the transistors is switched between the output and the power source by the number of arguments in the intercom. The argument included in the minterm without inversion controls the n-channel transistor, and the inverse argument is p-channel;

• the number of such consecutive connections corresponds to the number of minterms. Thus, the upper part of the circuit is constructed;

• complementary transistors are included between the output and the ground;

• each successive chain is supplemented by a parallel (and vice versa) circuit of transistors of opposite conductivity;

• the parallel links of complementary group inter themselves are included consistently

When constructing an inverse MDNF, the chains between the output signal and the power source, as well as the signal and the ground, change places.

5.4. Buffer Amplifiers

In order to provide a higher branching ratio at the output $K_{\text{раз}}$ without reducing the speed or increasing the power consumption from the power source in the n-MOS technology, special buffer amplifiers with inverting (or without inverting) the signal are used.

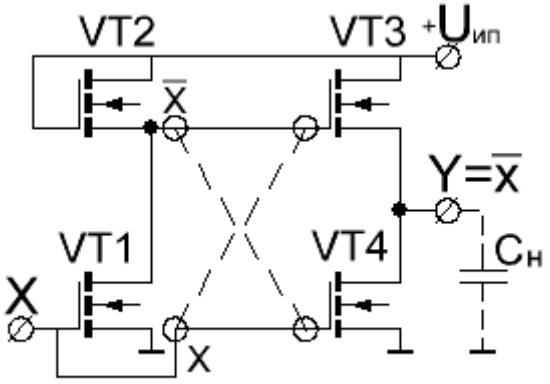


Fig 5.8

If the connections between the first cascade of the amplifier (transistors *VT1*, *VT2*) and the second (transistors *VT3*, *VT4*) are implemented by dashed lines, then a signal is formed as $Y = X$.

In case of realization of connections between cascades, the shown continuous lines are form a signal $\boldsymbol{Y} = \overline{\boldsymbol{X}}$.

The consumption current is determined from the expression $I_{\text{пот.}} = \frac{U_{\text{ип}}}{R_{i2}+R_{i1}}$ and may be very small, since the transistors with the parameters R_{i1}, $R_{i2} \gg R_{i3}$, R_{i4} are selected.

In a two-stage buffer amplifier, the first stage (transistors *VT1*, *VT2*) is an inverter with a high-level load in the *VT2* flow circuit, but with a low load capacity. The second cascade on transistors *VT3*, *VT4* is executed on a two-stage circuit and is controlled by phase-in signals from the input and output of the inverter. Therefore, the through current from the power supply $U_{\text{ип.}}$ through the transistors *VT3*, *VT4*, which in the open state (R_{i3}, R_{i4}) have low resistance, is excluded. As a result, with low current consumption (mainly due to the first cascade) buffer amplifiers provide an overload of equivalent load capacity through small resistance of transistors *VT3*, *VT4* in the open state. At the same time, the load capacity without loss of speed increases up to $K_{\text{раз.}} \leq 30$.

Duration of the output signal fronts:

$$t_{\text{ф}}^{01} = 3 \cdot \text{C}_{\text{н}} \cdot R_{i3},$$

$$t_{\text{ф}}^{10} = 3 \cdot \text{C}_{\text{н}} \cdot R_{i4}.$$

6. Integral injection logic Elements (I^2L)

6.1. Base element

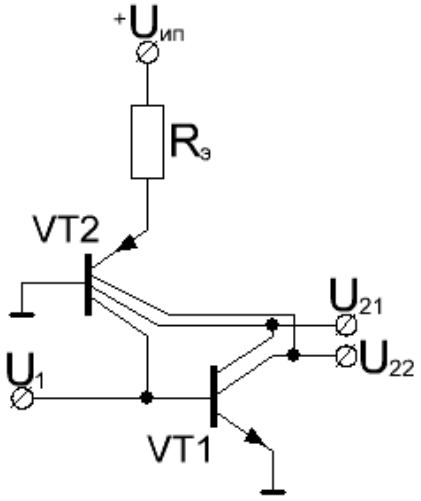
The desire of the developers of the elemental base to reduce the energy consumption and increase the degree of integration of logic elements on bipolar transistors, while maintaining their main advantage - high speed, led to the creation of integrated injecting logic (I^2L). Technology I^2L provides packing density of elements (more than 1000 elements per 1 mm^2), which exceeds the MOS technology. By power, the scattered I^2L elements can be compared with the CMOS while maintaining high-speed ($t_{зд.р} = 5\ ns$) inherent in bipolar integrated microcircuits.

The quality criterion of technology is the switching energy: the less energy, the better technology. For I^2L technology, this energy is:

$$W_K = P_{пот} \cdot t_{зд.р.ср} = 50 \cdot 10^{-12} J$$

The above advantages of the I^2L elements are achieved by the exception of the resistor circuits, which imply insignificant scattering power, the operation of bipolar transistors in unsaturated mode, small parasitic capacitances and a small difference in logical levels. Use in the I^2L elements of Schottky diodes allows you to increase the speed ($t_{зд.р} = 0.1 ns$) without increasing the power consumption.

The basic logic I^2L element (Fig. 6.1) contains the *p-n-p* transistor *VT2*, called the injector, which acts as a stable current sources I_K, and the multi-collector *n-p-n* transistor *VT1*, which performs the function of the inverter. The base type *n* transistor-injector is connected to the emitter type n transistor-inverter. Similarly, it was possible to combine the collector of the injector and the base of the inverter,



having conductivity type *p*.

Fig. 6.1

Transistor-injector *VT2* is constantly in active mode and the current in each of its *k* collectors is:

$$I_{\text{и}} = \frac{\alpha \cdot I_{\text{э}}}{k} = \frac{\alpha}{k} \cdot \frac{U_{\text{ип}} - U_{02}}{R_{\text{э}}} = const,$$

where U_{02} is threshold voltage for the emitter junctions of the transistor *VT2*, *k* - the number of collectors of the injection supply, $\alpha \approx 1$ - the coefficient of current transmission in the circuit with the general base. The input voltage determines the state of the emitter junction of the transistor *VT1*.

If the number of collectors k, then $I_{\text{э}}$ is evenly distributed over all k collectors.

When $U_1^1 > U_{01}$ (i.e., X = 1), the transistor VT1 is also open, voltage on its collectors equal

$U_{21} = U_{22} = U_{кн} = I_И \cdot r_{кн} = U_2^0$,

which responds to the value of the output logical variable Y = 0.

When $U_1^0 \leq U_{01}$ (i.e., X = 0), the transistor *VT1* is locked and voltage on its collectors equal

$$U_2^1 = I_u \cdot R_{\text{н}},$$

where $R_{\text{н}}$ is the load impedance. Most often, the load is the base of the next I^2L element. Then $U_2^1 > U_{\text{он}}$ So:

$$Y_1 = Y_2 = \overline{X}$$

6.1.1. Input characteristic (dependence $I_1 = f_1(U_1)$)

Input current of the I^2L element $I_1 = I_{\text{Б}} - I_{\text{И}}$, therefore the input characteristic of this element is the input characteristic of the bipolar transistor displaced by the Fig. 6.2 axis of currents by the magnitude $I_{\text{и}}$ (Fig. 6.2).

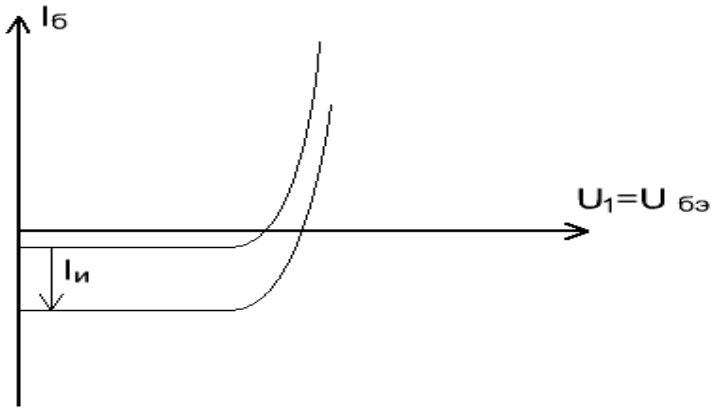


Fig.6.2

From the characteristics, it is clear that $I_1^0 \approx -I_И, I_1^1 \approx 0$. The logical voltage $\Delta U_1 = U_1^1 - U_1^0 = U_{Б.И.} - U_{К.Н.} \approx 0{,}6V$, difference is characterized by voltage levels at the closed and open emitter transistor *VT1*. Its temperature dependence determines the connection of the impedance of the I^2L circuits with the ambient temperature. When increasing temperature $U_{Б.И.}$ and ΔU_1 proportionally decreases and, accordingly, decreases stability.

6.1.2. Output characteristic

Output characteristic of the I^2L element (Fig. 6.3) in the mode of transistor cutoff *VT1* is the return current of the collector junction and does not depend on the output voltage, and in the open state, it is a line of saturation of collector characteristics. The current of the injector I_I flowing through the saturated resistance $r_{K.H.}$ transistor determines the output level of the logical zero. $U_2^0 \approx I_I r_{K.H.} = U_{K.Н.}$, and a high level at the output is formed when the current I_I flows through the load, that is, through the input circuit of the next element. Thus, the low level $U_1^0 = 0.05\,\text{V}$ at the input of the I^2L element responds to a high level $U_1^1 = 0.65\text{V}$ at its output, and vice versa, a high level at the input $U_1^1 = 0.65\,\text{V}$ responds to the level $U_2^0 = 0.05\text{V}$.O

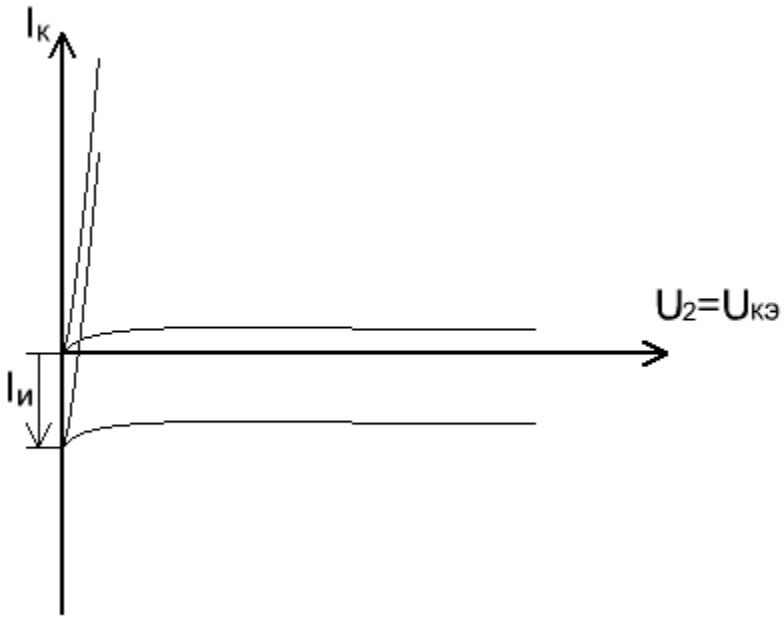


Fig. 6.3

On the characteristic, it is possible to construct a loading line, which is an input characteristic for other elements.

6.2. Realization of logical functions OR, NOR, AND, NAND

Logic functions in the I^2L technology are realized with the help of assembly of *n-p-n* transistor-inverter collectors.

In Fig. 6.4 shows circuit with two inputs and two outputs*:*

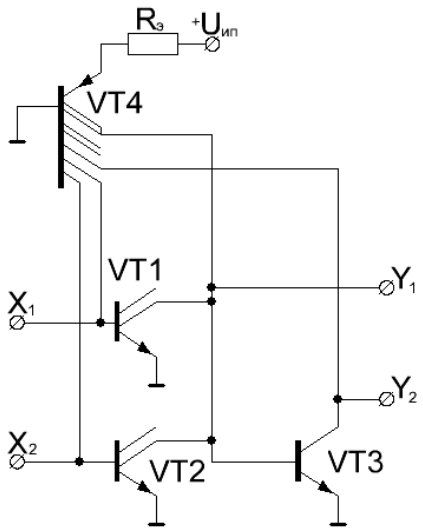


Fig. 6.4

The work of such a circuit is characterized by a table of states of outputs:

X_1	X_2	Y_1	Y_2
0	**0**	**1**	**0**
0	**1**	**0**	**1**
1	**0**	**0**	**1**
1	**1**	**0**	**1**

As can be seen from the table, the corresponding outputs implement the functions NOR (Y_1) and OR (Y_2):

$$Y_1 = \overline{X_1 + X_2}, Y_2 = \overline{Y_1} = X_1 + X_2$$

For the implementation of the basic logic AND, NAND we have to use additional inverters for input signals (Fig. 6.5). As can be seen from the circuit:

$$Y_3 = \overline{X' + X''} = \overline{\overline{X_1} + \overline{X_2}} = X_1 \cdot X_2, Y_4 = \overline{Y_3} = \overline{X_1 X_2}$$

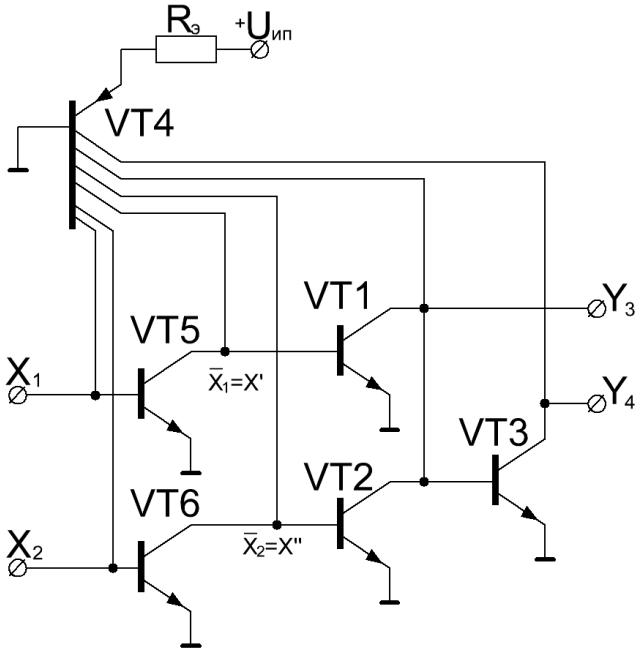


Fig. 6.5

Additional transistors in the path of the logic signal increase its delay, therefore, the logical elements AND, NAND in I^2L-technology are more inertial than the logical elements OR, NOR, and it is desirable to do without them for the development of high-speed circuits.

In Fig.6.6 shown an example of implementing the following function:

$$Y = \overline{\overline{X_1}X_2 + X_1\overline{X_2}} = X_1 \oplus X_2 = \overline{\overline{X_1 + X_2} + \overline{X_1 + X_2}} = (X_1 + X_2)(\overline{X_1} + \overline{X_2})$$

$$X' = \overline{X_1 + X_2}, X'' = \overline{\overline{X_1} + \overline{X_2}}, Y = \overline{X' + X''}, Y = X_1 \oplus X_2.$$

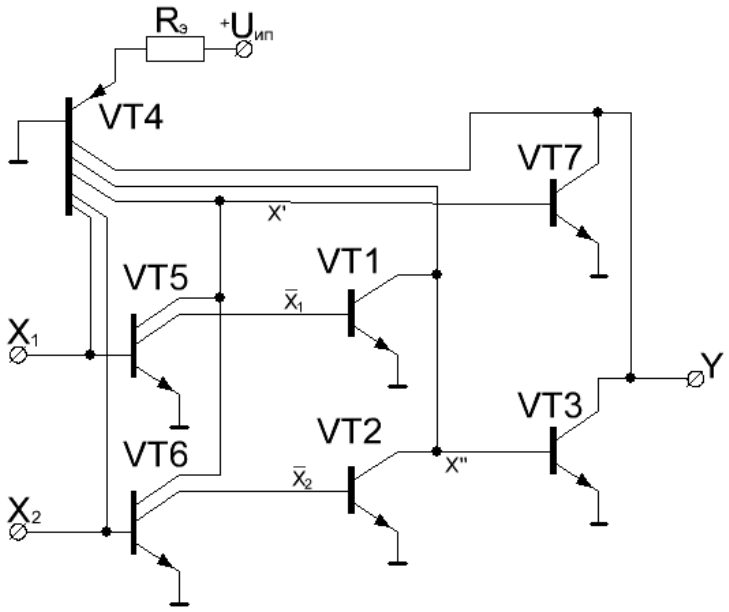


Fig.6.6

To implement an arbitrary function in the I^2L technology it is necessary:

• bring the implemented function to the minimum CNF;

• using a double inversion and de Morgan's theorem to express a function with the NOR operation;

• implement the NOR function by combining the collectors of transistors that are switched by a two-stage logical structure;

• determine the number of injection pump units and build an appropriate injection currents generator.

Consider an example that illustrates the sequence of synthesis operations for a logical combinational circuit for I^2L technology.

Let the function $Y\ (X_3, X_2, X_1, X_0)$ be given in the form of the perfect disjunctive normal form (PDNF):

$Y = (0,2,5,6,7,8,13,14,15)$.

We will find the MCNF:

X_3X_2 \ X_1X_0	00	01	11	10
00	1	0	0	1
01	0	1	1	1
11	0	1	1	1
10	1	0	0	0

$$= (X_2 + \overline{X_0})(\overline{X_2} + X_1 + X_0)(\overline{X_3} + X_2 + \overline{X_1})$$

Let's transfer the function to the basis NOR:

$$Y = \overline{(X_2 + \overline{X_0})(\overline{X_2} + X_1 + X_0)(\overline{X_3} + X_2 + \overline{X_1})}$$

$$= \overline{\overline{X_2 + \overline{X_0}} + \overline{\overline{X_2} + X_1 + X_0} + \overline{\overline{X_3} + X_2 + \overline{X_1}}} =$$

$$= \overline{X' + X'' + X'''}$$

The intermediate variables X ', X' ', X' " are realized by the basic elements NOR of the first stage, and the outputs of the first degree are arguments (inputs) of the second stage. In Fig. 6.7 is shown the synthesized circuit:

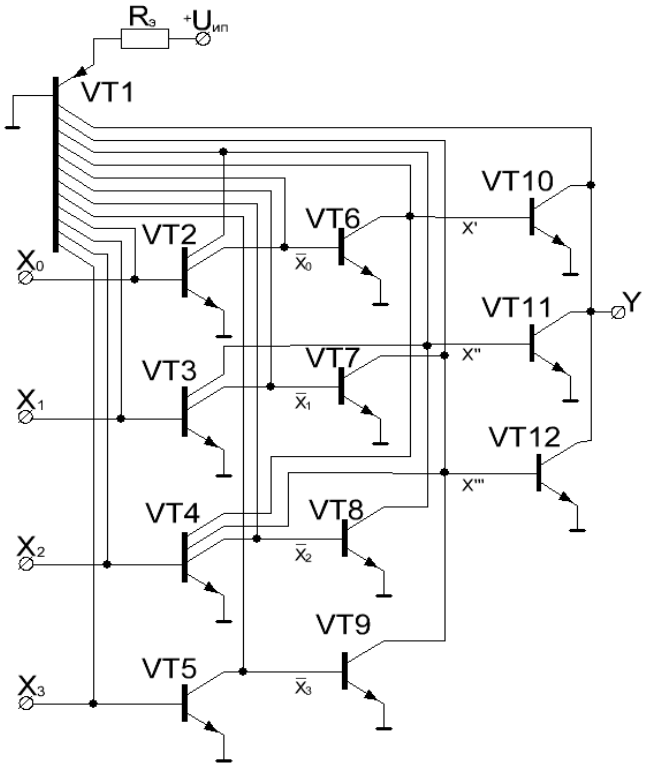


Fig.6.7

Checking the correctness of the circuit:

• all the bases of the transistors must have an injector supply;

• between any input and output, the signal must pass no more than 3 transistors.

7. Code Converters (CC)

Converters are designed to transfer codes submitting one form to another. For example, when entering information into computers successive should convert decimal numbers into binary, and the derivation of information on indicators or printers should binary or binary-coded decimal codes in turn control codes decoder, LED or LCD display panel, print engine.

7.1. Synthesis converter codes

May need to build a converter binary 3-bit gray code. Write a table of conformity:

Inputs			**Outputs**		
2^2	2^1	2^0	gray code		
X_2	X_1	X_0	Y_2	Y_1	Y_0
0	**0**	**0**	**0**	**0**	**0**
0	**0**	**1**	**0**	**0**	**1**
0	**1**	**0**	**0**	**1**	**1**
0	**1**	**1**	**0**	**1**	**0**
1	**0**	**0**	**1**	**1**	**0**
1	**0**	**1**	**1**	**1**	**1**
1	**1**	**0**	**1**	**0**	**1**
1	**1**	**1**	**1**	**0**	**0**

Each of the functions defined in a certain number of input variables. To find these functions and minimize Y_i use Karnaugh maps, writing in the cells Y value cards for each of the sets:

$Y_0 =$

X_2 \ X_1X_0	00	01	11	10
0	**0**	**1**	**0**	**1**
1	**0**	**1**	**0**	**1**

$$Y_0 = \overline{X_1}X_0 + X_1\overline{X_0} = (X_1 + X_0)(\overline{X_1} + \overline{X_0}) = X_1 \oplus X_0 = \overline{\overline{X_1}X_0 \cdot X_1\overline{X_0}} = \overline{\overline{X_1 + X_0} + \overline{X_1 + X_0}}$$

$Y_1 =$

X_2 \ X_1X_0	00	01	11	10
0	**0**	**0**	**1**	**1**
1	**1**	**1**	**0**	**0**

$$Y_1 = \overline{X_2}X_1 + X_2\overline{X_1} = X_1 \oplus X_2 = (X_2 + X_1)(\overline{X_2} + \overline{X_1}) = \overline{\overline{X_2}X_1 \cdot X_2\overline{X_1}} = \overline{\overline{X_2 + X_1} + \overline{X_2 + X_1}}$$

$Y_2 =$

X_2 \ X_1X_0	00	01	11	10
0	**0**	**0**	**0**	**0**
1	**1**	**1**	**1**	**1**

$$Y_2 = X_2$$

Variants converter code Gray binary code shown in Fig.7.1-7.3:

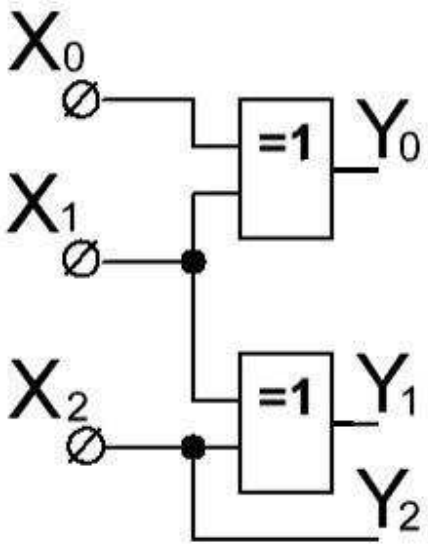


Fig.7.1

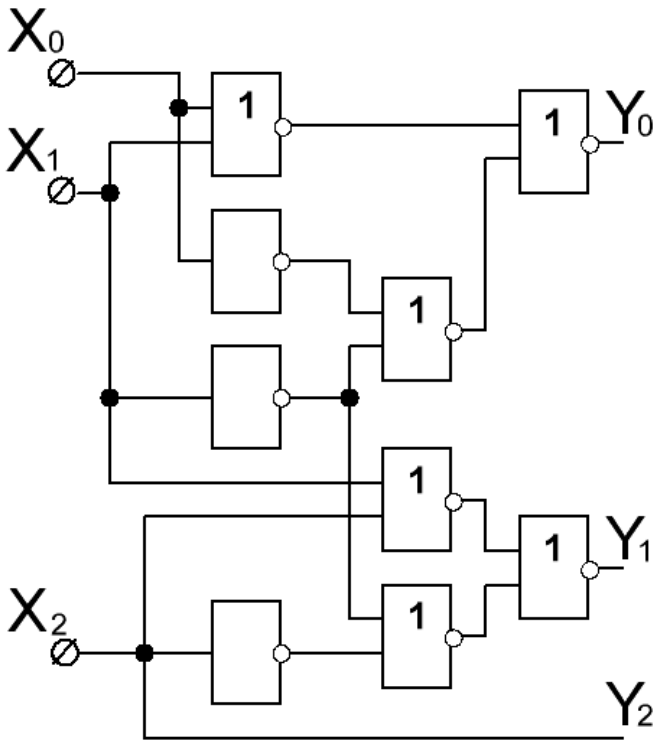


Fig.7.2

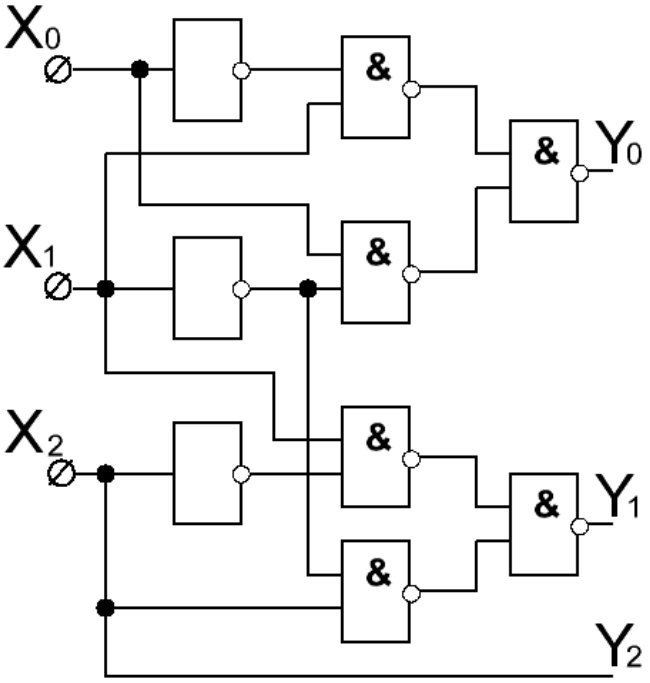
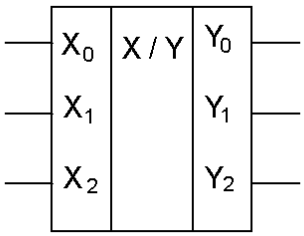


Fig.7.3

Qualified CC graphically depicted as follows:



For the synthesis of CC *n* -bit input code in the *m* -bit source, follow these steps:

- make a table matching the input and output codes;
- for each of the *m* outputs find MNDF, MCNF function of n input variables;
- using identical transformation MNDF and MCNF result obtained function to the form that is convenient for the joint implementation of a given technology;
- values obtained joint functions.

7.2. Encoder

A special case of a code converter is an encoder - this device provides the issuance of a certain code in response to the excitation of one of the inputs. Those. an encoder is a CC that converts a unitary code, or the code “1 of N”, into a code required by the conditions of the problem. In this case, N determines the number of inputs of the encoder.

Encoders are widely used to convert decimal numbers and alphabetic characters in binary code when entering information in computers and other digital devices. The encoder in the IMC type field is denoted by characters CD (CoDer).

Consider the example of building encoder to convert decimal numbers in code 8421. The input - a binary variable X_0 ... X_9, which are formed by pressing the corresponding switch input device. The variables are independent and can build 2^{10} = 1024 combinations of input, but if imposed restrictions prohibiting pressing two or more switches, then out of 1024 input combinations there are 10 valid. The input code corresponding to this limit is called unitary or code “1 of *N*”. Encoder in which all input variables have the same priority called non-priority. In our case, such variables $N = 10$.

X9	X8	X7	X6	X5	X4	X3	X2	X1	X0	Y3	Y2	Y1	Y0
0	0	0	0	0	0	0	0	0	1	0	0	0	0
0	0	0	0	0	0	0	0	1	0	0	0	0	1
0							1		0	0	0	1	0
0						1			0	0	0	1	1
0					1				0	0	1	0	0
0				1					0	0	1	0	1
0			1						0	0	1	1	0
0		1							0	0	1	1	1
0	1								0	1	0	0	0
1	0	0	0	0	0	0	0	0	0	1	0	0	1

Directly from the table can record the output function:

$$Y_0 = \overline{\overline{X_1 + X_3 + X_5 + X_7 + X_9}} = \overline{\overline{X_1} \cdot \overline{X_3} \cdot \overline{X_5} \cdot \overline{X_7} \cdot \overline{X_9}}$$

$$Y_1 = \overline{\overline{Y_2 + Y_3 + Y_6 + Y_7}} = \overline{\overline{X_2} \cdot \overline{X_3} \cdot \overline{X_6} \cdot \overline{X_7}}$$

$$Y_2 = \overline{\overline{X_1 + X_5 + X_6 + X_7}} = \overline{\overline{X_1} \cdot \overline{X_5} \cdot \overline{X_6} \cdot \overline{X_7}}$$

$$Y_3 = X_8 + X_9 = \overline{\overline{X_8} \cdot \overline{X_9}}$$

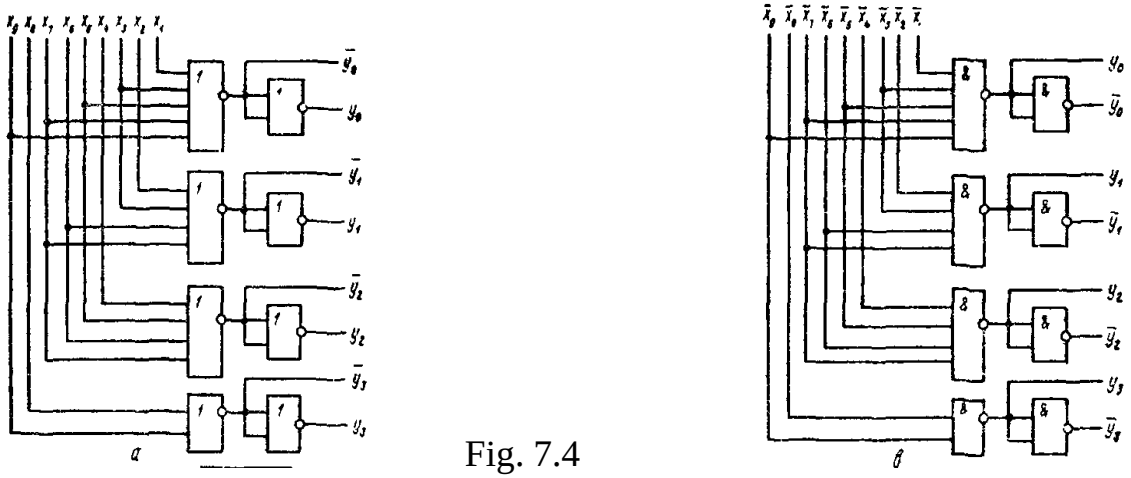


Fig. 7.4

In Fig.7.4 given encoder implementation on LE NOR (a) and NAND (б), and therefore conditional graphics:

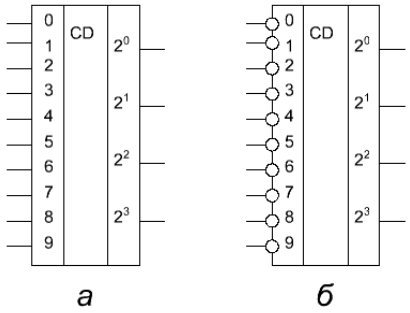


Fig. 7.5

The limit on the number of keys pressed often is unacceptable and need to build encoder so that while you press multiple switches he responded only to the oldest (or youngest) of them. Converters of this type of code called a priority encoder. They implement the conversion code "*k* of *N*" in the necessary code.

Consider the example of construction of a priority encoder "*k* of 10" in code "8421". The table according to priority encoder, in which the input variables with the highest number is the maximum priority values of input variables to the right of the diagonal 1 should not determine the source code:

X9	X8	X7	X6	X5	X4	X3	X2	X1	X0	Y3	Y2	Y1	Y0
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	*****	**0**	**0**	**0**	**1**
0	**0**	**0**	**0**	**0**	**0**	**0**	**1**	*****	*****	**0**	**0**	**1**	**0**
0	**0**	**0**	**0**	**0**	**0**	**1**	*****	*****	*****	**0**	**0**	**1**	**1**
0	**0**	**0**	**0**	**0**	**1**	*****	*****	*****	*****	**0**	**1**	**0**	**0**
0	**0**	**0**	**0**	**1**	*****	*****	*****	*****	*****	**0**	**1**	**0**	**1**
0	**0**	**0**	**1**	*****	*****	*****	*****	*****	*****	**0**	**1**	**1**	**0**
0	**0**	**1**	*****	*****	*****	*****	*****	*****	*****	**0**	**1**	**1**	**1**
0	**1**	*****	*****	*****	*****	*****	*****	*****	*****	**1**	**0**	**0**	**0**
1	*****	*****	*****	*****	*****	*****	*****	*****	*****	**1**	**0**	**0**	**1**

Priority encoder can be built based on non-priority encoder that converts code "1 of 10" in code "8421" when the pre-convert the input code "*k* of 10" to code "1 of 10".

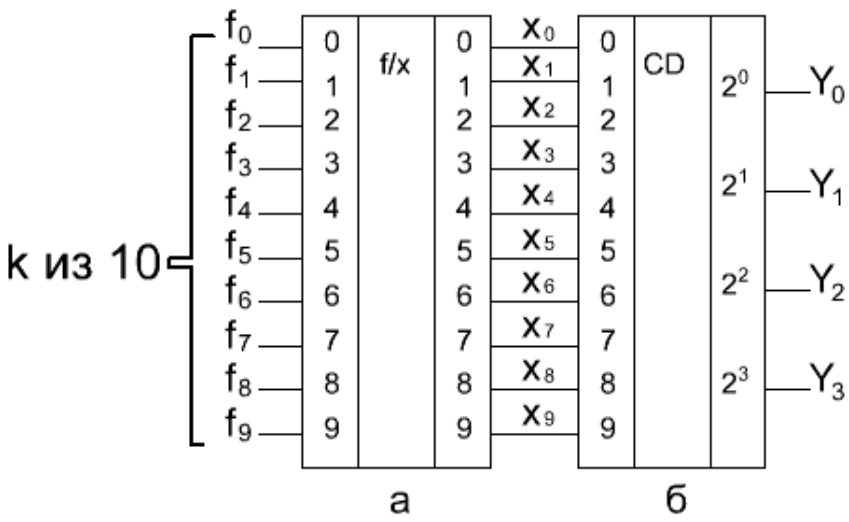


Fig. 7.6

Let the converter output variables "*k* of 10" to "1 of 10" through X_9, ..., X_0. Variable input f_9 has maximum priority, so do not depend on other input variables $X_9 = f_9$. Any other variable output X_i takes the value one if $f_i = 1$ and none of the "senior" inputs f_j, $j = \overline{i+1,9}$ not served logical unit, i.e.:

$$X_9 = f_9$$

$$X_8 = f_8 \cdot \overline{f_9}$$

$$X_7 = f_7 \cdot \overline{f_8} \cdot \overline{f_9} = f_7 \cdot \overline{f_8 + f_9}$$

$$X_6 = f_6 \cdot \overline{f_7} \cdot \overline{f_8} \cdot \overline{f_9} = f_6 \cdot \overline{f_7 + f_8 + f_9}$$

Similarly,

$$X_1 = f_1 \cdot \overline{f_2} \cdot \overline{f_3} \cdot \overline{f_4} \cdot \overline{f_5} \cdot \overline{f_6} \cdot \overline{f_7} \cdot \overline{f_8} \cdot \overline{f_9} = f_1 \cdot \overline{f_2 + ... + f_9}$$

$$X_0 = f_0 \cdot \overline{f_1} \cdot \overline{f_2} \cdot \overline{f_3} \cdot \overline{f_4} \cdot \overline{f_5} \cdot \overline{f_6} \cdot \overline{f_7} \cdot \overline{f_8} \cdot \overline{f_9} = f_0 \cdot \overline{f_1 + f_2 + ... + f_9}$$

Fig.7.7 shows scheme for realizing this transformation. Its advantage is the uniform propagation delay on all outputs and disadvantage - the need to use of multi-circuits NAND.

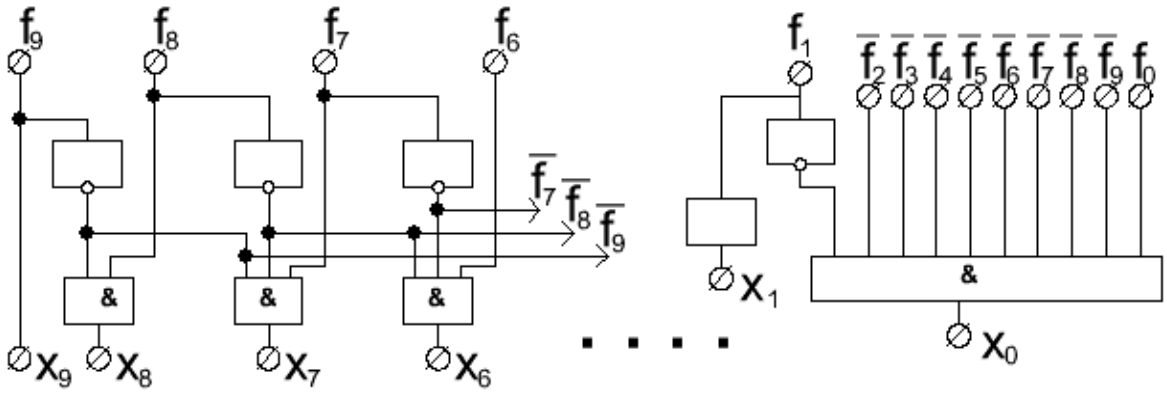


Fig. 7.7

If it is not imposed strict requirements for speed, e.g. keyboard, code converter "*k* of 10" to "1 of 10" can be done with less equipment (Fig.7.8).

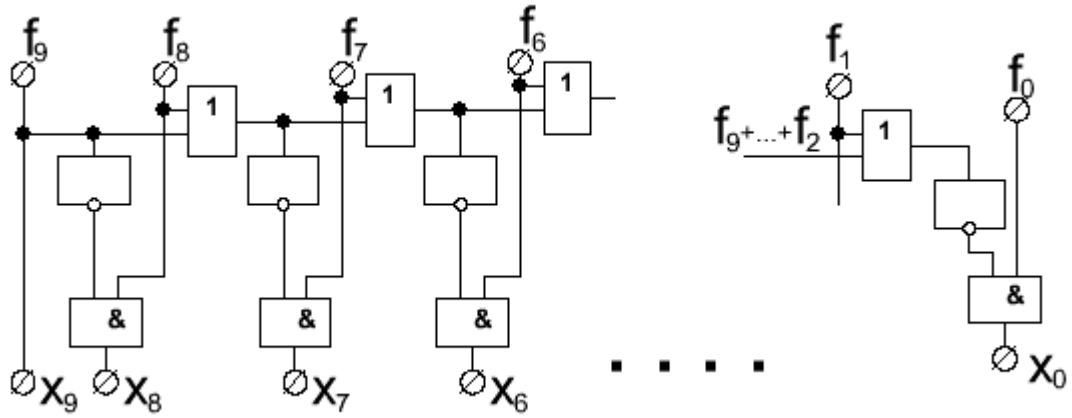


Fig. 7.8

In this scheme, signal priority prohibition applies to the older entry through junior series connected elements OR, because the whole duration of the conversion to code "1 of 10" is determined by the output X_0 maximum delay time settings.

7.3. Decoder

Convert any input code in the code "1 of *N*" converters perform code called decoder. The most widely used decoder targeted systems storage devices, information display devices from computers and other digital devices to external devices visualization and documentation of alphanumeric information. You need to give a signal "1 of *N*", such as cathode gas discharge indicator elements sample character printers and so on.

7.3.1. Linear decoder

Synthesis decoder structure, like any other converter codes beginning with writing table and matching input source.

Consider the example of transformation (decryption) binary code “8421” in a unitary code “1 of 10”.

“8421”				**“1 of 10”**	
X_3	X_2	X_1	X_0	Y	Minimization
0	**0**	**0**	**0**	$Y_0 = \overline{X_3} \cdot \overline{X_2} \cdot \overline{X_1} \cdot \overline{X_0}$	$= \overline{X_3 X_2 X_1 X_0}$
0	**0**	**0**	**1**	$Y_1 = \overline{X_3} \cdot \overline{X_2} \cdot \overline{X_1} \cdot X_0$	$= \overline{X_3 X_2 X_1} X_0$
0	**0**	**1**	**0**	$Y_2 = \overline{X_3} \cdot \overline{X_2} \cdot X_1 \cdot \overline{X_0}$	$= \overline{X_2} X_1 \overline{X_0}$
0	**0**	**1**	**1**	$Y_3 = \overline{X_3} \cdot \overline{X_2} \cdot X_1 \cdot X_0$	$= \overline{X_2} X_1 X_0$
0	**1**	**0**	**0**	$Y_4 = \overline{X_3} \cdot X_2 \cdot \overline{X_1} \cdot \overline{X_0}$	$= X_2 \overline{X_1 X_0}$
0	**1**	**0**	**1**	$Y_5 = \overline{X_3} \cdot X_2 \cdot \overline{X_1} \cdot X_0$	$= X_2 \overline{X_1} X_0$
0	**1**	**1**	**0**	$Y_6 = \overline{X_3} \cdot X_2 \cdot X_1 \cdot \overline{X_0}$	$= X_2 X_1 \overline{X_0}$
0	**1**	**1**	**1**	$Y_7 = \overline{X_3} \cdot X_2 \cdot X_1 \cdot X_0$	$= X_2 X_1 X_0$
1	**0**	**0**	**0**	$Y_8 = X_3 \cdot \overline{X_2} \cdot \overline{X_1} \cdot \overline{X_0}$	$= X_3 \overline{X_1}$
1	**0**	**0**	**1**	$Y_9 = X_3 \cdot \overline{X_2} \cdot \overline{X_1} \cdot X_0$	$= X_3 X_0$

N

m

Each output function need to Karnaugh map and use it to get it minimized expression.

X_3X_2 \ X_1X_0	00	01	11	10
00	**Y_0**	**Y_1**	**Y_3**	**Y_2**
01	**Y_4**	**Y_5**	**Y_7**	**Y_6**
11	*	*	*	*
10	**Y_8**	**Y_9**	*	*

If the number of inputs and m outputs *N* number of decoder related:

$$2^m = N,$$

then outputs defined for all sets and binary decoder called complete. At $2^m > N$ decoder called incomplete. Unused combinations (star map Carnot) to minimize the function exits.

Pictogram of the decoder shown in Fig.7.9-a, and its conditional pictogram on Fig.7.9-б.

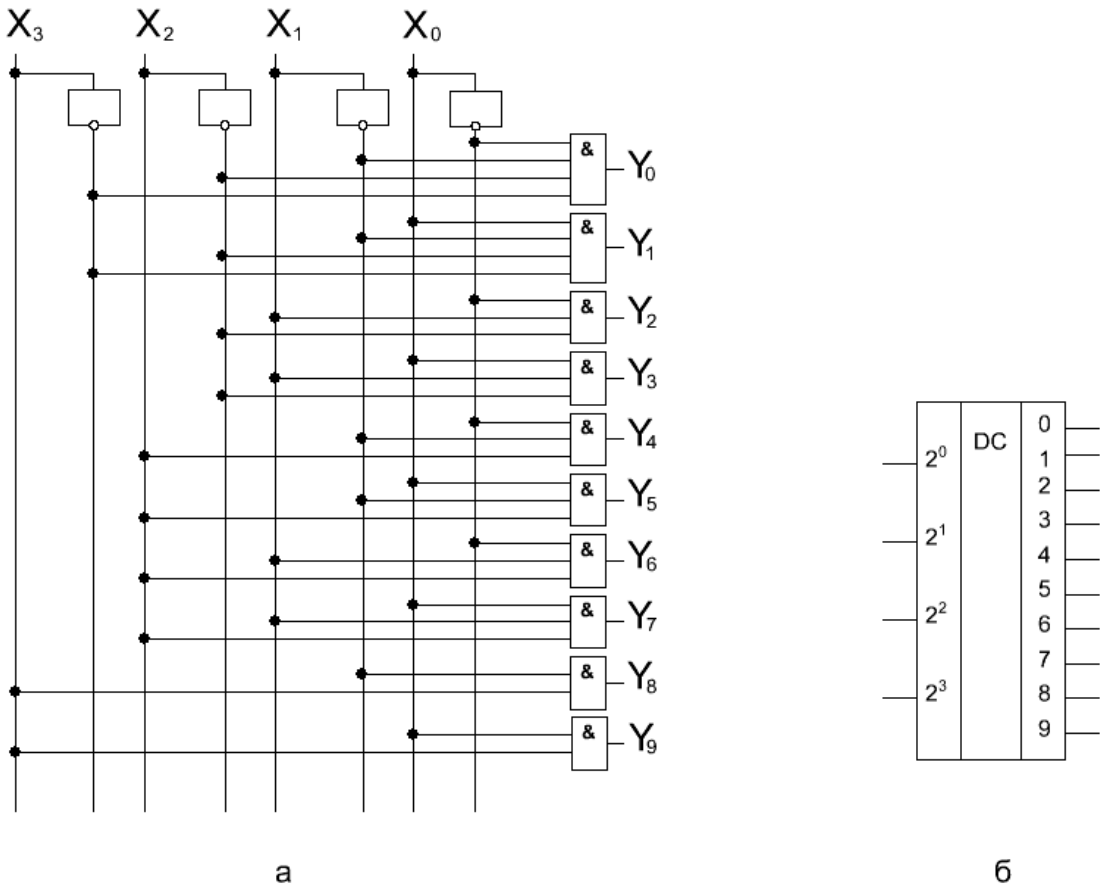


Fig. 7.9

This type is called linear decoder. They are characterized Single decryption input *m*-bit codes using m-post of the door logic elements. Linear decoder provides a conversion code with minimum delay and used in most high-speed digital circuits. However, with increasing bit input code m rapidly growing load each of the inputs and the number of buildings decoder IMCs to implement. The linear structure commonly used if $m \le 4$.

7.3.2. Pyramidal decoder

If the number of inputs $m > 4$ then to reduce the number of IMCs housings decoder performed by the multi-scheme. The first step pyramid decoder - a simple linear decoder with the number of outputs $n_1 = 4$ (Fig.7.10). Each successive level of driven more input variables, allows to double the number of exits and get $n_2 = 8, n_3 = 16$ etc., i.e. *k*-step full pyramidal decoder has a number of outputs $N = 2^{K+1}$, and $k = m - 1$.

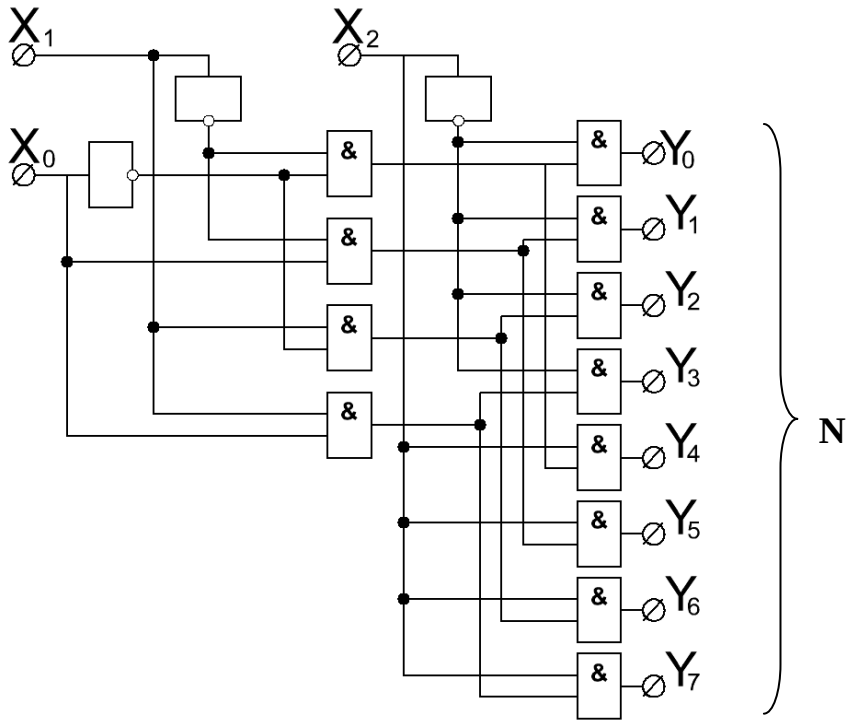


Fig. 7.10

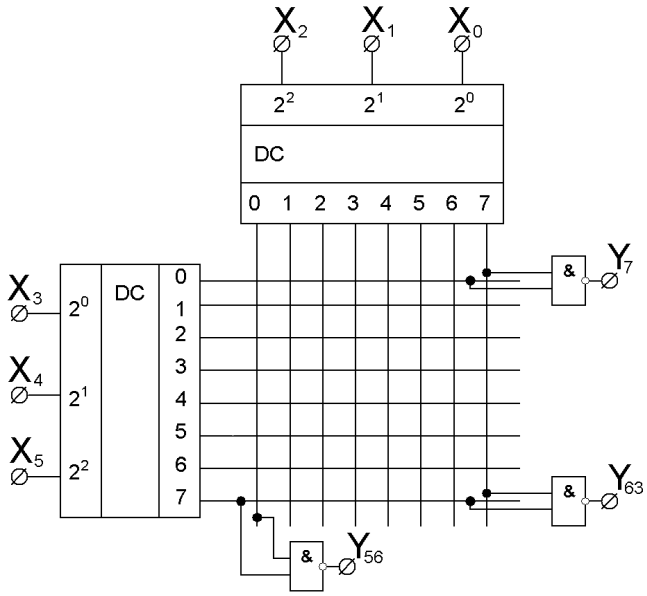
The advantage is a regular structure are similar dual-input elements.

The disadvantage of such decoder are delay proportional to the number of digits, uneven load inputs, which increases with the number of stages.

7.3.3. Matrix decoder

If the number of inputs $m \geq 5$, it is better to build decoder on a matrix structure. When paired *m* number of rows and columns of the matrix is $2^{m/2}$ and matrix output valves Square comes. At odd m input variables divided into $\frac{m-1}{2}$ and $\frac{m+1}{2}$.

In both cases, selection rows and columns (Fig.7.11), in which nodes are connected dual-input valves, as well as row and column decoder used linear or pyramidal decoder. This type is called decoder or rectangular matrix.



Their advantage is that they provide a relatively small delay as the linear decoder and regular structure.

Fig. 7.11

7.4. Multiplexers

In digital devices often need to transfer digital information from various devices m to n receivers through a public channel. For this inlet channel, setting device called a multiplexer which, in accordance with the code for A_m channel connects to one of the m sources. To connect inputs x_i is set to release a single table that case $m = 4$ looks like:

A_1	A_0	**Y**
0	**0**	X_0
0	**1**	X_1
1	**0**	X_2
1	**1**	X_3

Address inputs A_0, A_1show which of the inputs X_0, X_1, X_2, X_3 must be connected to the output *Y*.

Inputs X_0, X_1, X_2, X_3 assign *addresses* and thus set the working condition of the switch. Then adopted addressing output function for the example is as follows:

$$Y = \overline{A_1} \cdot \overline{A_0} \cdot X_0 + \overline{A_1} \cdot A_0 \cdot X_1 + A_1 \cdot \overline{A_0} \cdot X_2 + A_1 \cdot A_0 \cdot X_3 =$$

$$= \overline{\overline{\overline{A_1} \cdot \overline{A_0} \cdot X_0} \cdot \overline{\overline{A_1} \cdot A_0 \cdot X_1} \cdot \overline{A_1 \cdot \overline{A_0} \cdot X_2} \cdot \overline{A_1 \cdot A_0 \cdot X_3}}$$

We have MDNF that requires *minimization*. We can present it in basis NAND or NOR. Realization on the elements NOR shown in Fig.7.12.

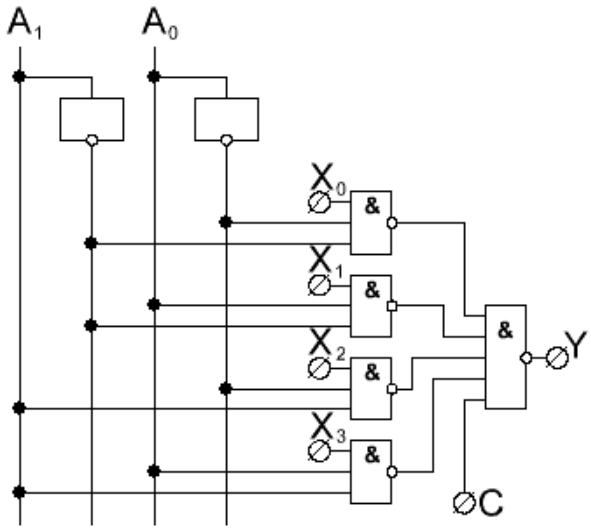


Fig. 7.12

Here: $X_0. \ldots X_3$- information inputs, A_0, A_1- address, name entry that can be connected, *C* - gating input (optional).

Gating input required to disable the output of the multiplexer at the time of change of address to prevent unauthorized connection release (random) input signals.

If *C = 1*: *Y = f (A, X)*, and when *C = 0*, *Y = 1*.

At the time we submit a change of address *C* = 0, currently locked out because yak.ne depends on the information inputs.

In Fig.7.13 are conventionally pictogram multiplexer

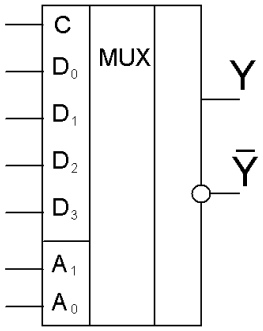


Fig. 7.13

Since select one of *N* inputs, it is advisable to use a decoder. The signals control the decoder logic switches, allowing transmission of information via only one of them. While this scheme will look like multiplexer (Fig.7.14):

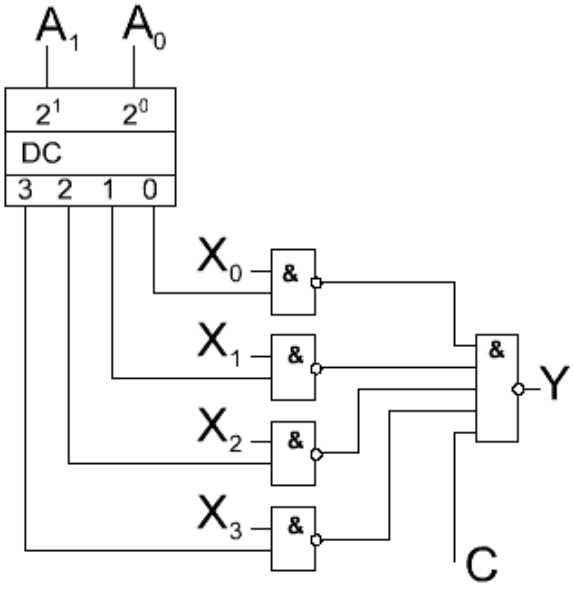


Fig. 7.14

Consider some use Schematic multiplexers. It is obvious to use multiplexer as the transducer parallel m-bit binary code consistent. It's enough to give the inputs of the multiplexer parallel code and then gradually change the address code in the required sequence. However, to avoid false signal multiplexer output strobe pulse for switching addresses must disable output of inputs.

Multiplexers can be used to build logic functions of several variables in a disjunctive normal form.

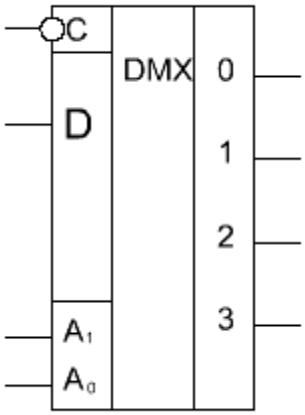
7.5. Demultiplexer

Demultiplexer - combinational devices that implement data bus connecting a single input to one of the *N* outputs according to address code (i.e. “1 of *N*”). Demultiplexer includes an address decoder.

Demultiplexer logic operation for the case $N = 4$ is given in the table below.

A_1	A_0	***X***
0	**0**	$Y_0 = x \cdot \overline{A_1} \cdot \overline{A_0}$
0	**1**	$Y_1 = x \cdot \overline{A_1} \cdot A_0$
1	**0**	$Y_2 = x \cdot A_1 \cdot \overline{A_0}$
1	**1**	$Y_3 = x \cdot A_1 \cdot A_0$

A qualified graphic image demultiplexer:



Simple demultiplexer scheme that implements the specified conversion table is shown in Fig.7.15

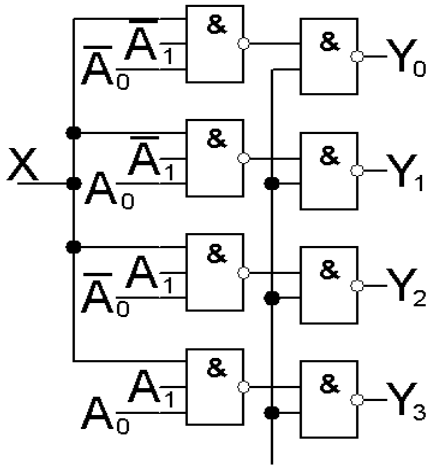


Fig. 7.15

Demultiplexer can also build based on decoder. The scheme of the demultiplexer is shown in Fig.7.16.

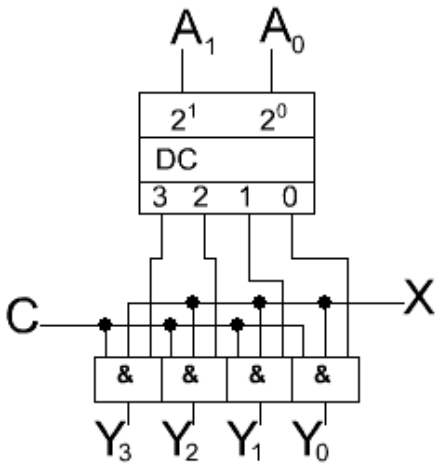


Fig. 7.16

7.6. Realization of logic functions multiplexers

Multiplexers can be used to build logic functions of several variables in a disjunctive normal form.

Let set general view multiplexer functions:

$$Y_M = \overline{A_1} \cdot \overline{A_0} \cdot D_0 + \overline{A_1} \cdot A_0 \cdot D_1 + A_1 \cdot \overline{A_0} \cdot D_2 + A_1 \cdot A_0 \cdot D_3$$

As an example, take some function:

$$Y = X_3 \cdot \overline{X_2} \cdot \overline{X_1} + \overline{X_3} \cdot X_2 \cdot \overline{X_1} + \overline{X_3} \cdot \overline{X_2} \cdot X_1 + X_3 \cdot X_2 \cdot X_1$$

and we realize it on multiplexer.

We can assign one input variable information, and others - address. So identify $A_1 = X_2$, $A_0 = X_0$ then a comparison with expressions minterms Y_M and Y follows: $D_0 = X_3$, $D_1 = \overline{X_3}$, $D_2 = \overline{X_3}$, $D_3 = X_3$

Multiplexers build on this feature:

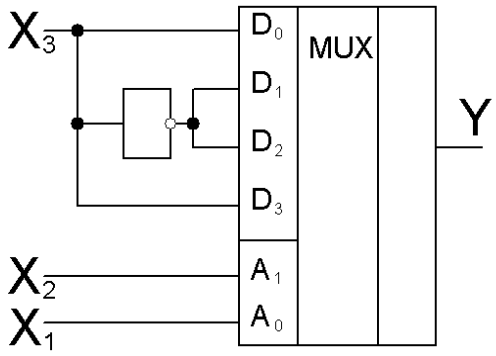


Fig. 7.17

If we use multiplexer with 2 information inputs, then this function can be represented as:

$$Y = \overline{X_3} \cdot (X_2 \cdot \overline{X_1} + \overline{X_2} \cdot X_1) + X_3 \cdot (\overline{X_2} \cdot \overline{X_1} + X_2 \cdot X_1)$$

For 2-inputs multiplexer, output function is:

$$Y_M = \overline{A} \cdot D_0 + A \cdot D_1$$

If $A = X_3$ then a comparison Y_M and Y follows:

$$D_0 = X_2 \cdot \overline{X_1} + \overline{X_2} \cdot X_1 = X_2 \oplus X_1, \; D_1 = \overline{X_2} \cdot \overline{X_1} + X_2 \cdot X_1 = \overline{X_2 \oplus X_1}$$

Realization of functions *Y* on 2-inputs multiplexer shown in Fig.7.18.

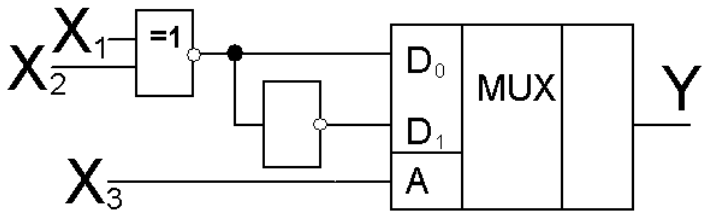


Fig. 7.18

Synthesis of logic devices based multiplexer can be formalized.

The algorithm synthesis device for realization logic based multiplexer includes the following:

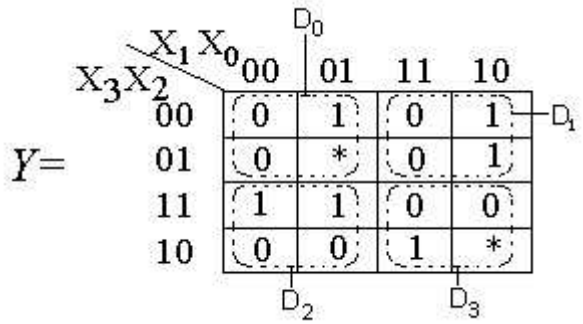
- To obtain MDNF, fill a given function Karnaugh map (or Veitch diagram).
- Karnaugh map should highlight areas by the number of multiplexer inputs information that we use. The variables that retain their values within the selected area is targeted for a multiplexer, and the rest - information.
- Each region must find minimal information on the form variables to control information multiplexer inputs.
- With identical shape are minimal changes to the form convenient for joint implementation.
- Implementation of schemes for each information input multiplexer.

Consider as an example the synthesis of logic device that implements the function $Y(X_3, X_2, X_1, X_0) = (1, 2, 5^*, 6, 10^*, 11, 12, 13)$. In parentheses are the decimal equivalents of binary numbers X_3, X_2, X_1, X_0. That is $1100_2 = 12_{10}$, which responds minterm $\overline{X_3}\,\overline{X_2}\,\overline{X_1}X_0$. Similarly $2_{10} \rightarrow \overline{X_3}\,\overline{X_2}\,X_1\overline{X_0}$, $6_{10} \rightarrow \overline{X_3}\,X_2\,X_1\overline{X_0}$ and so on. For data sets of arguments the function takes the value 1. Numbers with an asterisk means that these sets of arguments feature vague, i.e. sets of arguments $\overline{X_3}X_2\overline{X_1}X_0 = *$ and $X_3\overline{X_2}X_1\overline{X_0} = *$ Y functions can be assigned any value that simplifies implementation.

- Step 1:

$$Y = \overline{X_3}\,\overline{X_2}\,\overline{X_1}X_0 + \overline{X_3}\,\overline{X_2}\,X_1\overline{X_0} + \overline{X_3}X_2\overline{X_1}X_0^{\,*} + \overline{X_3}\,X_2\,X_1\overline{X_0} + X_3\overline{X_2}X_1\overline{X_0}^{\,*} + X_3\overline{X_2}X_1X_0 + X_3X_2\overline{X_1}\,\overline{X_0} + X_3X_2\overline{X_1}X_0$$

- Step 2:



- Step 3:

For 4-inputs information multiplexer, Karnaugh map divide into 4 address areas so that address will be variables X_3 and X_1. Assign value $A_1 = X_3$, A_0

= X_1. Then the numbers of address areas respond to the targeted areas shown on the Karnaugh map.

- Step 4:

  Find the management functions of each information input of multiplexer:

  $D_0 = X_0;\ D_1 = \overline{X_0};\ D_2 = X_2;\ D_3 = \overline{X_2}.$

- Step 5:

  In this case, no conversion is needed.

- Step 6:

  Building a scheme that implements a given function $Y(X_3, X_2, X_1, X_0)$:

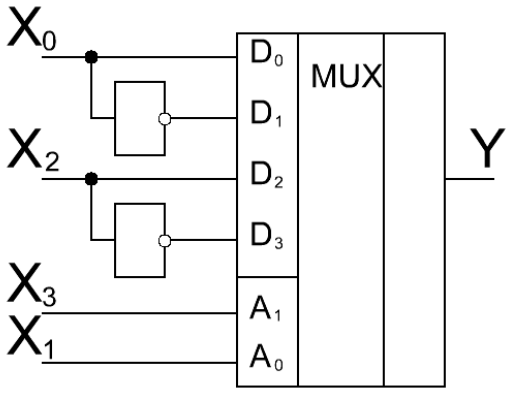


Fig. 7.19

7.7. Combination devices shift

The need to shift the digital data occurs, when the numbers are normalized, performing arithmetic operations on them, etc. If for one working cycle necessary to shift by only one digit to the left or right, then this operation, combining it with the function of storing information conveniently performed using shift registers to trigger. Where a single cycle shift must perform an arbitrary number of digits in either direction, convenient to use combinational logic device based multiplexers. Number of multiplexers required is equal to the output bit binary number.

Starting to build a table shifting device that communicates address code multiplexer that connects to each of their outputs discharge numbers shift. Bit address code multiplexer p determines the maximum possible number of shift per clock cycle: $\Delta S_{\max} = 2^p - 1$.

Suppose you want to build a combinational device that adjusts shift according to the table:

Address		**The outputs of the shift device**			
A_1	A_0	Y_3	Y_2	Y_1	Y_0
0	**0**	X_3	X_2	X_1	X_0
0	**1**	X_2	X_1	X_0	X_{-1}
1	**0**	X_1	X_0	X_{-1}	X_{-2}
1	**1**	X_0	X_{-1}	X_{-2}	X_{-3}

If a combinational device shift numbers carried left, with senior level lost. Imagine this unit shift as a set of multiplexers, each of which forms a discharge source:

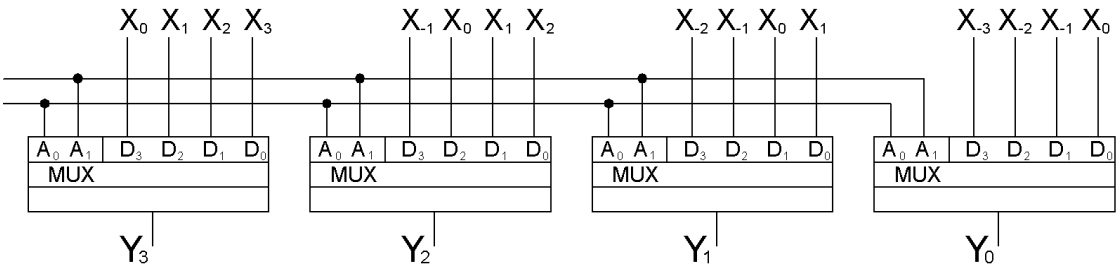


Fig. 7.20

This option is Y_0, Y_1, Y_2, Y_3; all address inputs are combined and controlled variables simultaneously $A_1 = 0$, $A_0 = 0$.

If $A_1 = 0$, $A_0 = 0$, The outputs are connected to inputs D_0.

If $A_1 = 0$, $A_0 = 1$ (Shift by one digit), the output Y_i to appear X_i the inputs D_1.

If $A_1 = 1$, $A_0 = 0$ (Shift of two bits) Y_i there are signals of the inputs D_2.

And when $A_1 = 1$, $A_0 = 1$ respectively, offset by 3 bits and outputs Y_i connected to inputs D_3 multiplexers.

Alternating bits can be in any order, which is an important advantage multiplexer.

Conventionally, a graphic representation of the Raman shift device (bullpen) shown in Fig.7.21.

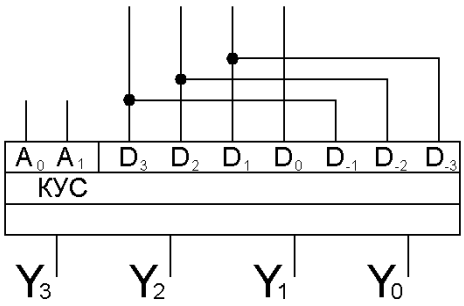


Fig.7.21

Advantages:

- In combinational device shift performed on any number of bits per clock cycle (it depends on the sequence in which to switch addresses).
- Very simply chosen direction of displacement
- During the shift could easily modify the code shift.

Drawback*:* is a complicated device.

8. Combinational adders (CA)

Combinational adders are designed to perform arithmetic operations of addition and subtraction of single-and multi-numbers (operands). Multi- digit adder consists according numbers of single-digit adders.

8.1. Half adders

Single-digit adder whose input received two single-digit numbers A and B, and the output is also generated single-digit number S and transfer amount and carry P, called half adder. That half adder is a device which implements arithmetic addition of two single-digit binary numbers.

The truth table for half adder can record feature amount calculation unit S and transfer overcrowding P in the most significant bit (MSB):

A	B	P	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

$$S = \overline{A} \cdot B + A \cdot \overline{B} = A \oplus B = \overline{A \cdot B + \overline{A} \cdot \overline{B}} = \overline{\overline{\overline{A} \cdot B} + \overline{A \cdot \overline{B}}} = \overline{\overline{\overline{A} \cdot \overline{B}} + \overline{A \cdot B}}$$
$$= \overline{P + \overline{A + B}}$$

$$P = A \cdot B = \overline{\overline{A} + \overline{B}}$$

Implementation half adder based on identical transformations is shown in Fig.8.1 and Fig.8.2.

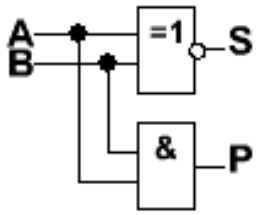


Fig. 8.1.

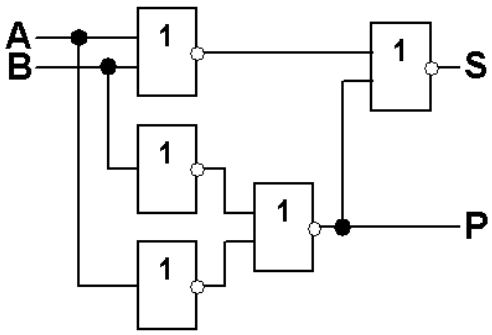


Fig. 8.2.

Conditionally half adder graphic is displayed as shown in Fig.8.3:

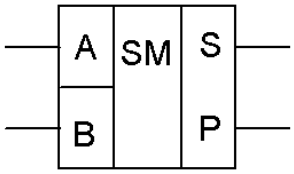


Fig. 8.3

8.2. Full adders

If single-adder implements the addition of three single-items A, B, C and thus forms the feature amounts S and P transfer function, it is called full adder. Full adder described by the following table:

A	***B***	***C***	***P***	***S***
0	**0**	**0**	**0**	**0**
0	**1**	**0**	**0**	**1**
1	**0**	**0**	**0**	**1**
1	**1**	**0**	**1**	**0**
0	**0**	**1**	**0**	**1**
0	**1**	**1**	**1**	**0**
1	**0**	**1**	**1**	**0**
1	**1**	**1**	**1**	**1**

Find the features MDNF amount of *S* & *P* and transport together carry some options. The Karnaugh Map for the three variables *A*, *B*, *C*:

***P* =**

$\mathbf{X_2}$ \ $\mathbf{X_1X_0}$	00	01	11	10
0	**0**	**0**	**1**	**0**
1	**0**	**1**	**1**	**1**

$$P = A \cdot B \cdot \overline{C} + \overline{A} \cdot B \cdot C + A \cdot B \cdot C + A \cdot \overline{B} \cdot C = C \cdot (\overline{A} \cdot B + A \cdot \overline{B}) + A \cdot B =$$

$$= C \cdot S' + A \cdot B = \overline{\overline{C \cdot S'} \cdot \overline{A \cdot B}}, S' = \overline{A} \cdot B + A \cdot \overline{B}$$

$S =$

X_2 \ X_1X_0	00	01	11	10
0	**0**	**1**	**0**	**1**
1	**1**	**0**	**1**	**0**

$$S = \overline{A} \cdot B \cdot \overline{C} + A \cdot \overline{B} \cdot \overline{C} + \overline{A} \cdot \overline{B} \cdot C + A \cdot B \cdot C$$

$$= \overline{\overline{\overline{A} \cdot B \cdot \overline{C}} \cdot \overline{A \cdot \overline{B} \cdot \overline{C}} \cdot \overline{\overline{A} \cdot \overline{B} \cdot C} \cdot \overline{A \cdot B \cdot C}} =$$

$$= \overline{C} \cdot (\overline{A} \cdot B + A \cdot \overline{B}) + \mathrm{C} \cdot (\overline{A} \cdot \overline{B} + A \cdot B) = \overline{C} \cdot S' + \mathrm{C} \cdot \overline{S'} = C \oplus S'$$
$$= C \oplus A \oplus B$$

Realization of this adder on element NAND shown in Fig.8.5:

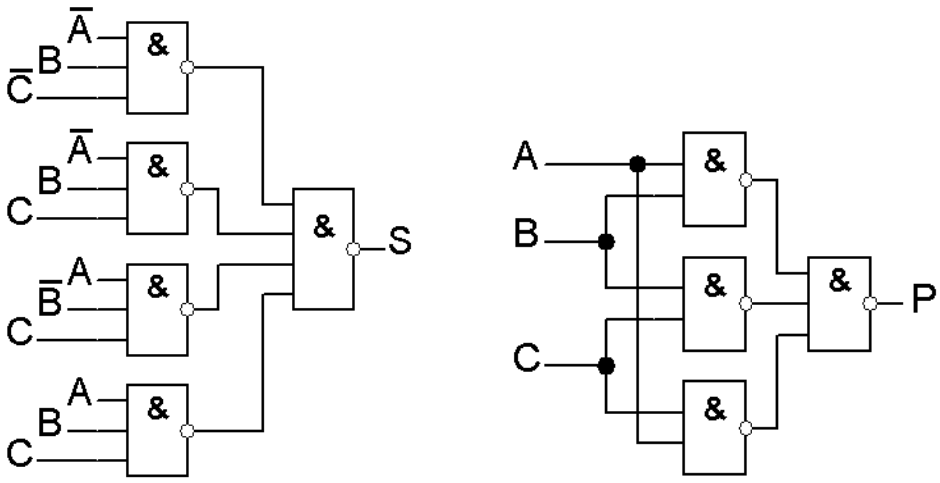


Fig. 8.5.

Conditionally pictogram full adder shown in Fig.8.6:

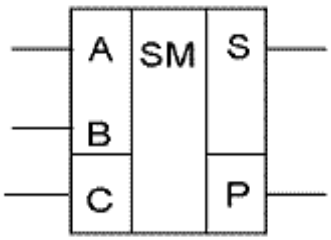


Fig. 8.6.

Adder circuit elements on the EXCLUSIVE OR and NAND represented on Fig.8.7:

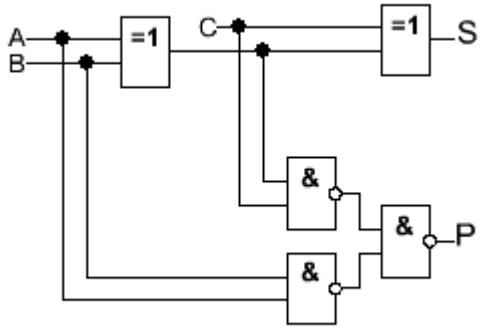


Fig. 8.7.

Advantage circuit using logical elements exclusive OR and NAND is easy implementation. A disadvantage - a significant delay in the output of exclusive OR elements.

8.3. Subtractor

Subtractor is a device that implements the subtraction of two single-digit numbers A_i, B_i and borrow from LSB of $V_{i-1}$with forming of difference signals D_i and borrow V_i of MSB. Let needed from A_i subtract B_i and V_{i-1} where V_{i-1} borrow unit of the MSB:

$$\begin{array}{r} \_A_i \\ \_B_i \\ V_{i-1} \\ \hline V_i D_i \end{array}$$

Then the possible values for feature differences D_i and functions borrow $V_i$defined below truth table. According to the truth table subtractor write the expression for the difference D_i and functions borrow V_i:

A	B	V_{i-1}	V_i	D_i
0	**0**	**0**	**0**	**0**
0	**1**	**0**	**1**	**1**
1	**0**	**0**	**0**	**1**
1	**1**	**0**	**0**	**0**

0	**0**	**1**	**1**	**1**
0	**1**	**1**	**1**	**0**
1	**0**	**1**	**0**	**0**
1	**1**	**1**	**1**	**1**

Then the function numbers the difference is:

$D_i=$

$\mathbf{V_{i-1}}$ \ $\mathbf{A_i B_i}$	00	01	11	10
0	**0**	**1**	**0**	**0**
1	**1**	**1**	**1**	**0**

$$D_i = \overline{A_i} \cdot B_i \cdot \overline{V_{i-1}} + A_i \cdot \overline{B_i} \cdot \overline{V_{i-1}} + \overline{A_i} \cdot \overline{B_i} \cdot V_{i-1} + A_i \cdot B_i \cdot V_{i-1} =$$

$$= \overline{V_{i-1}} \cdot (\overline{A_i} \cdot B_i + A_i \cdot \overline{B_i}) + V_{i-1}(\overline{A_i} \cdot \overline{B_i} + A_i \cdot B_i) =$$

$$= \overline{V_{i-1}} \cdot S' + V_{i-1} \cdot S' = V_{i-1} \oplus S' = V_{i-1} \oplus A_i \oplus B_i.$$

Function borrow V_i:

$V_i=$

$\mathbf{V_{i-1}}$ \ $\mathbf{A_i B_i}$	00	01	11	10
0	**0**	**1**	**0**	**0**
1	**1**	**1**	**1**	**0**

$$V_i = \overline{A} \cdot B \cdot \overline{V_i} + \overline{A} \cdot \overline{B} \cdot V_i + \overline{A} \cdot B \cdot V_{i-1} + A \cdot B \cdot V_{i-1} =$$

$$= V_{i-1} \cdot (\overline{A} \cdot \overline{B} + A \cdot B) + \overline{A} \cdot B = \overline{\overline{V_i \cdot \overline{S'}} \cdot \overline{\overline{A} \cdot B}}$$

Using identical expressions for D_i and V_i we can realize the full single-digit subtractor with different element bases.

Scheme of such subtractor on elements NAND and EXCLUSIVE OR is shown in Fig.8.8:

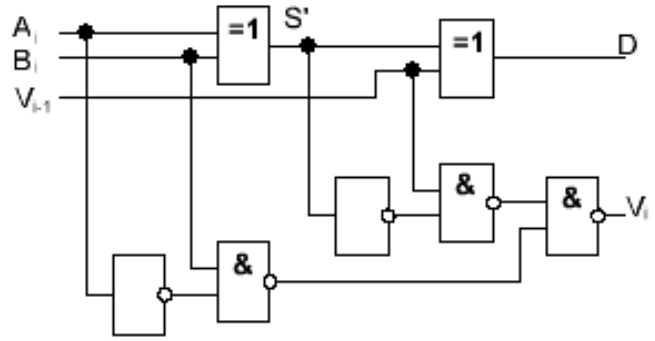


Fig. 8.8.

A comparison of expressions S_i and D_i shows that $S_i \equiv D_i$. Therefore, subtractor can build on a full adder, replacing subtracted numbers in reverse compiling code:

$$\begin{array}{r} A_i \\ +\overline{B}_i \\ +\overline{V_{i-1}} \\ \hline P_i^* S_i^* \end{array}$$

For such an operation truth table is:

A	$\overline{B}$	$\overline{V_{i-1}}$	P^*	S_i^*
0	**1**	**1**	**1**	**0**
0	**0**	**1**	**0**	**1**
1	**1**	**1**	**1**	**1**
1	**0**	**1**	**1**	**0**
0	**1**	**0**	**0**	**1**
0	**0**	**0**	**0**	**0**
1	**1**	**0**	**1**	**0**
1	**0**	**0**	**0**	**1**

Comparing the value functions P_i^*, S_i^* with V_i and D_i tables for subtractor and adder can be noted that $P_i^* = \overline{V_i}$, $S_i^* = D_i$. Therefore the output of the adder transfers P_i^* necessary to invert.

This subtractor based on adder shown in Fig.8.9:

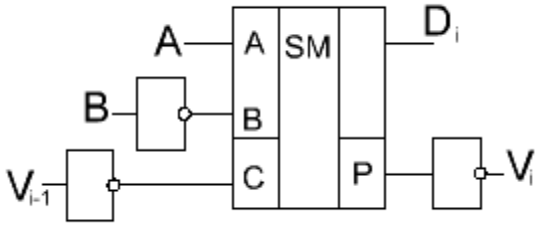


Fig. 8.9.

8.4. An algebraic adder

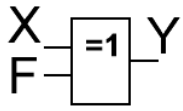
An algebraic adder can be used to add or subtract as necessary. The combination of addition and subtraction operations need additional signal *F*, which sets the mode combiners using controlled inverter:

$$Y = \begin{cases} X, F = 0 \\ \overline{X}, F = 1 \end{cases},$$

where *F*- control signal.

As such controlled inverter can be used EXCLUSIVE OR element:

$$Y = X\overline{F} + \overline{X}F$$



If $F = 0$, we have $Y = X$ without inversion signal transmission, while $F = 1$ we have inversion of the input signal on output: $Y = \overline{X}$.

Such circuit of algebraic adder shown in Fig.8.10

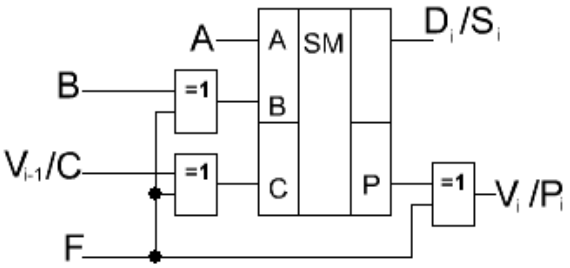


Fig. 8.10

At $F = 0$ device performed the operation of addition of A_i, B_i, C_i and became sum S_i and transfer P_i. While $F = 1$ device performed the operation of subtraction and became difference V_i and borrow D_i.

8.5. Multi-bitadder

Adder of the two multi-bit numbers can be implemented using single-bit adders. So can be realized the consecutive or parallel adder.

Suppose you want to add two 4-bit numbers A and B:

$$\begin{array}{r} A_4A_3A_2A_1 \\ +\ B_4B_3B_2B_1 \\ \hline P_4S_4S_3S_2S_1 \end{array}$$

Scheme of consecutive addition of the transfer P_i is shown in Fig.8.11:

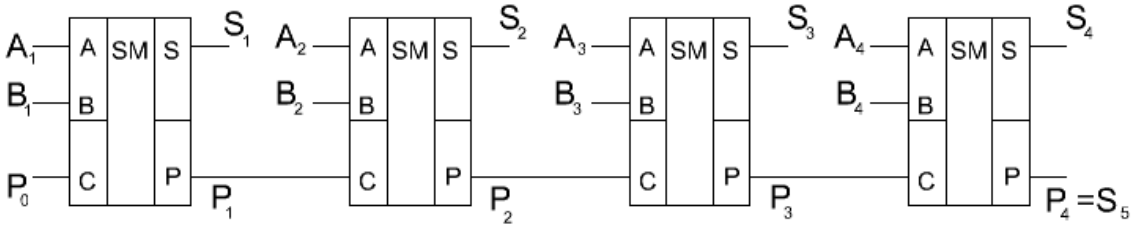


Fig. 8.11

Consecutive adder requires minimal equipment costs. However, the time of adding is proportional number bit of operands. By delay duration unit transfer as serial adder can be used in the relatively slow operating digital devices.

Cycle duration T of serial adder is proportional to n bits adder and time of delay of the transfer in one single-digit adder $t_{зд.р.п.}$:

$$T = n.\, t_{зд.р.п.}$$

In parallel m-bit adder amount of each bit, S_i defined as the logical sum 2i + 1 arguments. Therefore, the complexity of implementing output functions rapidly increases with the number output level. In addition, equipment costs are rising rapidly with increasing bit operands. Cycle duration T and complexity of realization of parallel adder depend on how the unit of the transfer would bring.

To construct a parallel circuit transfer function we introduce a notation function of transparency $A_i \oplus B_i = H_i$ and function of generating transfer $A_i \cdot B_i =$

G_i. Using the tool transparencyH_i and generating functions G_i for any output bit of adder can write:

$$S_i = A_i \oplus B_i \oplus P_{i-1} = H_i \oplus P_{i-1},$$

$$P_i = A_i \cdot B_i + (A_i \oplus B_i)P_{i-1} = G_i + H_i P_{i-1}.$$

Based on these ratios can write:

$S_1 = H_1 \oplus P_0,\ P_1 = G_1 + P_0 H_1$

$S_2 = H_2 \oplus P_1,\ P_2 = G_2 + P_1 H_2 = G_2 + G_1 H_2 + P_0 H_1 H_2$

$S_3 = H_3 \oplus P_2,\ P_3 = G_3 + P_2 H_3 = G_3 + G_2 H_3 + G_1 H_2 H_3 + P_0 H_1 H_2 H_3$

$S_4 = H_4 \oplus P_3,\ P_4 = G_4 + P_3 H_4 = G_4 + G_3 H_4 + G_2 H_3 H_4 + G_1 H_2 H_3 H_4 + P_0 H_1 H_2 H_3 H_4.$

That is, each of the outputs the multi-bit adder can be recorded as DNF of the functions of generation and transparency. In this case, all output variables S_1, S_2, S_3, S_4 and $P_4 = S_5$ are calculated simultaneously. This ensures minimum delay its conclusions, and therefore the highest speed.

Parallel transfer scheme the more complex, the more arguments defining feature.

Section of 4-bit adder graphically is shown in Fig.8.12.

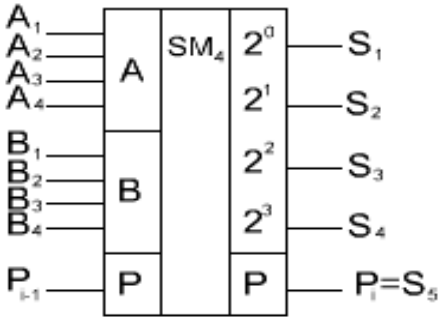


Fig. 8.12

The complexity of parallel transfer scheme rapidly increases with the number of bits adder, therefore multi-combiners are often divided into sections, which are implemented in parallel transfer. Between sections the transfer sections can be implemented consistently. The best find multi-bit adder division into 4-bit sections.

In the presence of 4-bit sections, the multi-number operand *A* can divided into tetrads:

$$\begin{array}{l} A_8A_7A_6A_5 \quad A_4A_3A_2A_1 \\ + \qquad\qquad + \\ B_8B_7B_6B_5 \quad B_4B_3B_2B_1 \\ + \qquad\qquad + \\ \qquad P_4 \qquad\qquad P_0 \\ \hline P_8 \;\; S_8\,S_7S_6S_5 \;\; P_4\,S_4S_3S_2S_1 \end{array}$$

Scheme of connection sections adder with serial transfer between the sections shown in Fig.8.13:

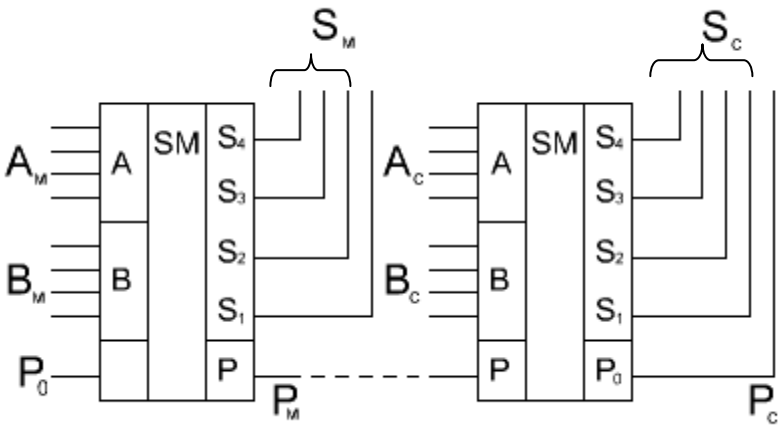


Fig. 8.13

8.6. Binary-coded decimal adder

The calculator, device registration and conversion of digital information, represented in decimal form, commonly used arithmetic devices with binary-coded decimal operands.

The basic element of a decimal adder may be 4-bit binary adder section that should realize the addition of two decimal digits k-th level: $A_{K4}A_{K3}A_{K2}A_{K1}$ and $B_{K4}B_{K3}B_{K2}B_{K1}$ considering transfer $P_{k-1}$of previous tetrads (k-1)-th decimal places. At the exit k-th section must be the result amounts $S_{K4}S_{K3}S_{K2}S_{K1}$ and transfer P_k to a tetrad (*k + 1*)-th decimal places.

The table shows the values S_i' and P_i' derived when adding binary-decimal numbers (tetrads) using binary adder sections and values S_i,P_i, which will ultimately be received.

Σ_{10}		2^4	2^3	2^1	2^0	***Binary-coded decimal***					Σ_{10}
	P'	S'_4	S'_3	S'_2	S'_1	P	S_4	S_2	S_3	S_1	
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
1	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**1**
2	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**0**	**2**
3	**0**	**0**	**0**	**1**	**1**	**0**	**0**	**0**	**1**	**1**	**3**
4	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**4**
5	**0**	**0**	**1**	**0**	**1**	**0**	**0**	**1**	**0**	**1**	**5**
6	**0**	**0**	**1**	**1**	**0**	**0**	**0**	**1**	**1**	**0**	**6**
7	**0**	**0**	**1**	**1**	**1**	**0**	**0**	**1**	**1**	**1**	**7**
8	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**8**
9	**0**	**1**	**0**	**0**	**1**	**0**	**1**	**0**	**0**	**1**	**9**
10	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**0**	**16**
11	**0**	**1**	**0**	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**17**
12	**0**	**1**	**1**	**0**	**0**	**1**	**0**	**0**	**1**	**0**	**18**
13	**0**	**1**	**1**	**0**	**1**	**1**	**0**	**0**	**1**	**1**	**19**
14	**0**	**1**	**1**	**1**	**0**	**1**	**0**	**1**	**0**	**0**	**20**
15	**0**	**1**	**1**	**1**	**1**	**1**	**0**	**1**	**0**	**1**	**21**
16	**1**	**0**	**0**	**0**	**0**	**1**	**0**	**1**	**1**	**0**	**22**
17	**1**	**0**	**0**	**0**	**1**	**1**	**0**	**1**	**1**	**1**	**23**
18	**1**	**0**	**0**	**1**	**0**	**1**	**1**	**0**	**0**	**0**	**24**
19	**1**	**0**	**0**	**1**	**1**	**1**	**1**	**0**	**0**	**1**	**25**

As the table, shows summing binary-decimal operands giving sum $S'_{K4}S'_{K3}S'_{K2}S'_{K1}$ and transferP'_K, which starting from the 10-th row do not respond to the addition of decimal numbers. In lines 16…19 need only correction of sum, and in lines 10…15 - the sum and transfer. Correction must convert the sum $S'_{K4}S'_{K3}S'_{K2}S'_{K1}$ in the sum $S_{K4}S_{K3}S_{K2}S_{K1}$ and transfer P'_K in P_k.

Correction of transfer is performed by logical adding:

$$P_K = P_K{}' + P_{\text{cor}},$$

where P_{cor} - corrective term, that is set to logical “1” on sets $S'_{K4}S'_{K3}S'_{K2}S'_{K1}$ 10-15 lines of the table, that is:

$S'_4S'_3$ \ $S'_2S'_1$	00	01	11	10
00	**0**	**0**	**0**	**0**
01	**0**	**0**	**0**	**0**
11	**1**	**1**	**1**	**1**
10	**0**	**0**	**1**	**1**

$$P_{\text{cor}} = = S'_4 \cdot S'_3 + S'_4 \cdot S'_2.$$

Then $P_K = P'_K + P_{\text{cor}} = \overline{P'_K + S'_4 \cdot S'_3 + S'_4 \cdot S'} = \overline{\overline{P'_K} \cdot \overline{S'_4 \cdot S'_3} \cdot \overline{S'_4 \cdot S'}}.$

The need of correction result is always arises in P_K= 1. In this case, to get the correct result should to intermediate result $S'_{K4}S'_{K3}S'_{K2}S'_{K1}$ add code $0110_2 = 6_{10}$, that is:

$\Sigma_{2-10} = \Sigma_2 + P(0110)_2$- (binary-coded decimal binary + number of 6 to 10 combinations).

Implementation of section binary-decimal adder based on two sections of the binary adder shown in Fig.8.14:

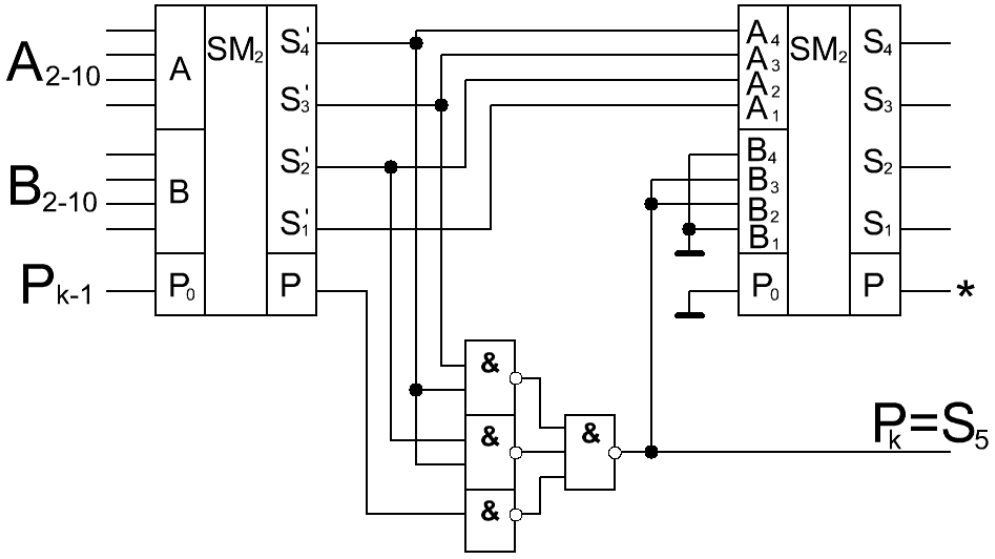


Fig. 8.14

8.7. Combinational Multiplier

Due to the high speed, combinational adders are widely used in various devices handling digital information. One possible application is the multiplication unit based on combinational adders.

Let we need multiply of two binary numbers $A_4A_3A_2A_1$ and$B_4B_3B_2B_1$. To take product $\Pi_8\Pi_7\Pi_6\Pi_5\Pi_4\Pi_3\Pi_2\Pi_1$ need do arithmetic multiplication:

				A_4	A_3	A_2	A_1
				B_4	B_3	B_2	B_1
				A_4B_1	A_3B_1	A_2B_1	A_1B_1
			A_4B_2	A_3B_2	A_2B_2	A_1B_2	
		A_4B_3	A_3B_3	A_2B_3	A_1B_3		
	A_4B_4	A_3B_4	A_2B_4	A_1B_4			
Π_8	Π_7	Π_6	Π_5	Π_4	Π_3	Π_2	Π_1

Here products of the type A_iB_j determined using conjunction of relevant variables.

Multiplication of two numbers *A* and *B* can be done using the addition and shift. Some works are uniquely determined by multiplying number $A_4A_3A_2A_1$for the next bit B_i multiplier *B*. Each subsequent single product must shift by one digit compared to the previous. The final product comes with sequential addition of intermediate products.

Implementation multiplier based on the single-digit adders shown in Fig.8.15:

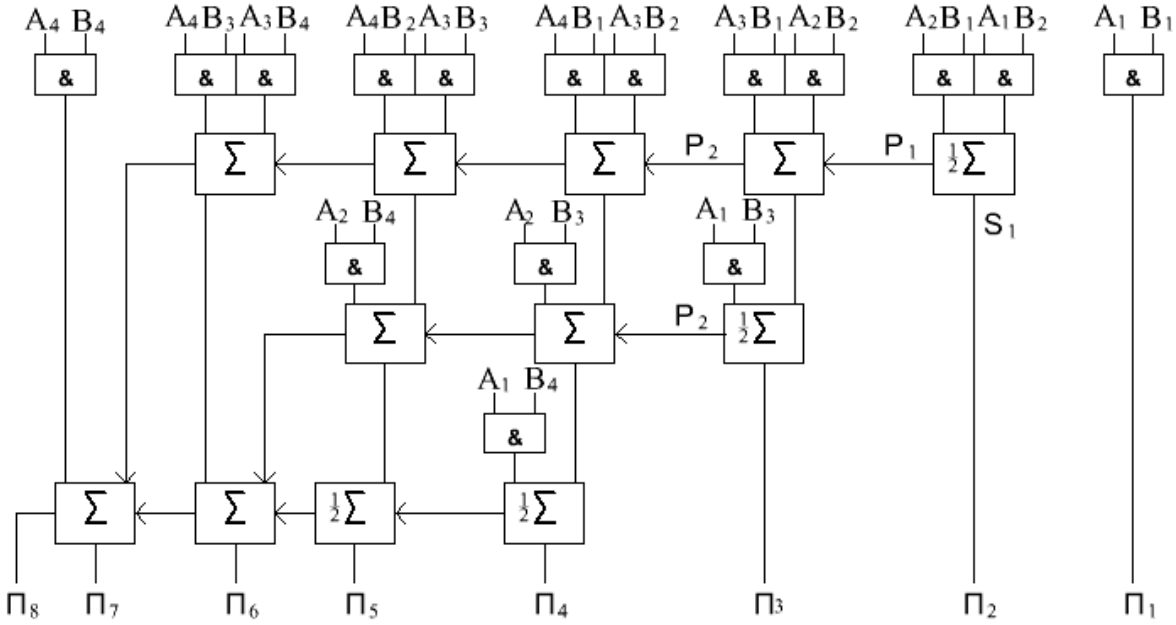


Fig. 8.15

The main advantage of combinational multiplier is high speed, which is not related to clock synchronization device and determined only by the signal delay in the logic elements.

Combination multipliers can be used effectively in the construction of digital filters to perform the necessary calculations of fast Fourier transform in microprocessor systems.

9. Digital comparators

Comparator - a combinational device that performs the functions of the ratio of two or more operands (code combinations that are involved in arithmetic expressions).

For two operands A and B are functions:

$$F(A > B) = \overset{>}{F}, \; F(A < B) = \overset{<}{F}, \; F(A = B) = \overset{=}{F}$$

and their superposition: $F(A \geq B) = \overset{\geq}{F}$, $F(A \leq B) = \overset{\leq}{F}$.

Most importantly comparator detects equality arguments that A = B. Universal comparator must identify all possible related arguments.

9.1. Single-bit digital comparator

Functions of the relationship between single-bit operands are presented in the table below:

A	***B***	$\overset{>}{F}$	$\overset{=}{F}$	$\overset{<}{F}$	$\overset{\geq}{F}$	$\overset{\leq}{F}$
0	**0**	**0**	**1**	**0**	**1**	**1**
0	**1**	**0**	**0**	**1**	**0**	**1**
1	**0**	**1**	**0**	**0**	**1**	**0**
1	**1**	**0**	**1**	**0**	**1**	**1**

The functions $\overset{>}{F}$, $\overset{<}{F}$, $\overset{=}{F}$ can be realized as follows:

$$\overset{>}{F} = A \cdot \overline{B} = \overline{\overline{A} + B},$$

$$\overset{<}{F} = \overline{A} \cdot B = \overline{A + \overline{B}},$$

$$\overset{=}{F} = \overline{A} \cdot \overline{B} + A \cdot B = A \sim B = \overline{A \oplus B} = \overline{\overline{A} \cdot B + A \cdot \overline{B}} = \overline{\overline{\overline{A} \cdot \overline{B}} \cdot \overline{A \cdot B}} = \overline{\overset{>}{F} + \overset{<}{F}}.$$

On fig.9.1-a, б are presented some realization that matched logical expressions, and on the fig.9.1-в - pictogram of one-bit comparator.

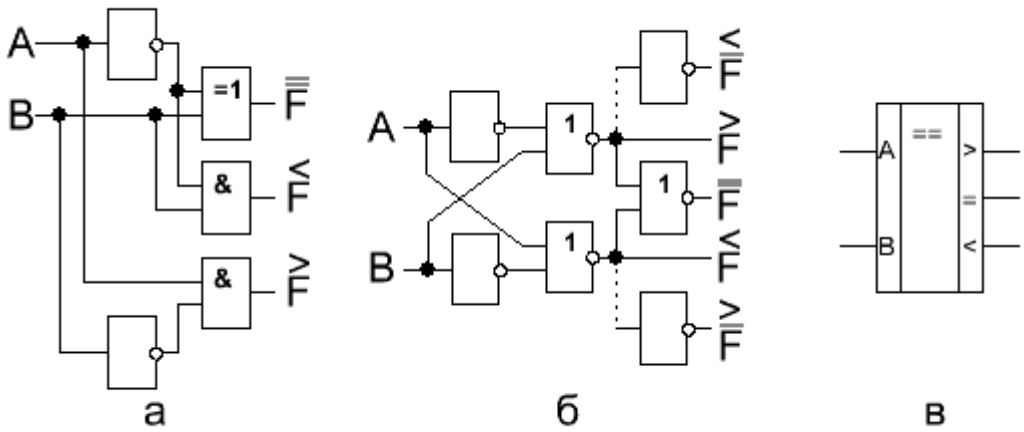


Fig. 9.1

9.2. Multi-bit digital comparator

Suppose there are a 3-binary number $A_3A_2A_1$, Compare it with the number $B_3B_2B_1$. Then we get the relation for =, > and <,:

$$\overset{=}{F}_3 = (A_3 = B_3)\cdot(A_2 = B_2)\cdot(A_1 = B_1) = (\overline{A_3 \oplus B_3})\cdot(\overline{A_2 \oplus B_2})\cdot(\overline{A_1 \oplus B_1}) =$$
$$= \overline{(A_3 \oplus B_3) + (A_2 \oplus B_2) + (A_1 \oplus B_1)}$$

$$\overset{>}{F}_3 = (A_3 > B_3) + (A_2 = B_2)\cdot(A_2 > B_2) + (A_3 = B_3)\cdot(A_2 = B_2)\cdot(A_1 > B_1) =$$
$$= A_3 \cdot \overline{B_3} + (A_3 \cdot B_3 + \overline{A_3} \cdot \overline{B_3})(A_2 \cdot \overline{B_2} + (A_2 \cdot B_2 + \overline{A_2} \cdot \overline{B_2}) \cdot A_1 \cdot \overline{B_1}) =$$
$$= \overline{\overline{A_3} \cdot B_3} + (\overline{A_3} \oplus B_3)(\overline{\overline{A_2} + B_2} + (\overline{A_2} \oplus B_2) \cdot \overline{\overline{A_1} + B_1})$$

The realization of these functions $\overset{>}{F}_3$ and $\overset{=}{F}_3$ shown on Fig.9.2 and Fig.9.3:

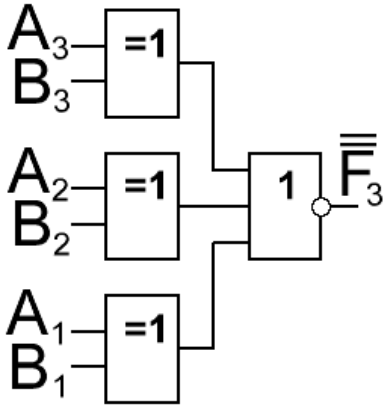


Fig. 9.2

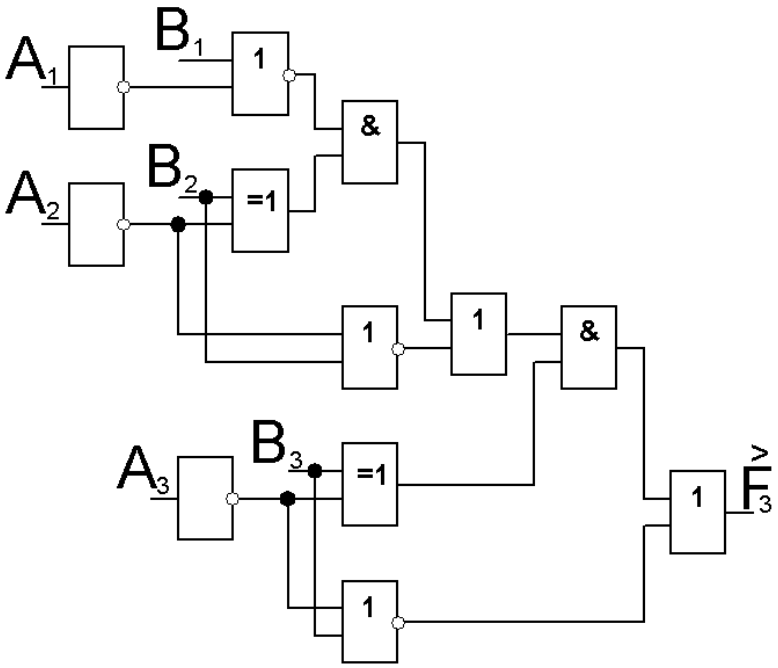


Fig. 9.3

As seen from the scheme, the delay signal $\overset{>}{F}_3$ is proportional to the number of digits that are compared. To decrease delay time of output signal functions $\overset{>}{F}_3$, $\overset{<}{F}_3$ should lead to the kind of DNF (CNF) and minimized.

After minimization for $\overset{>}{F}_3$ we get expressions:

$$\overset{>}{F}_3 = A_3 \cdot \overline{B_3} + A_3 \cdot A_2 \cdot \overline{B_2} + \overline{B_3} \cdot A_2 \cdot \overline{B_2} + A_3 \cdot A_1 \cdot \overline{B_2} \cdot \overline{B_1} + A_3 \cdot A_2 \cdot A_1 \cdot \overline{B_1} + A_2 \cdot A_1 \cdot \overline{B_3} \cdot \overline{B_1} + A_1 \cdot \cdot \overline{B_3} \cdot \overline{B_2} \cdot \overline{B_1}$$

The logical scheme of functions $\overset{>}{F}_3$ is shown on fig.9.4. This scheme provides a minimum delay output signal and therefore maximum performance. Scheme for realization function $\overset{<}{F}_3$ will be similarly, if the relevant variables A_i and B_i to swap.

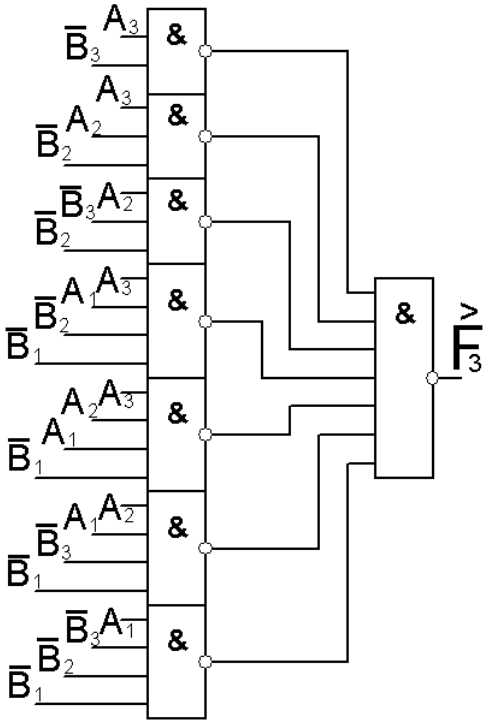


Fig. 9.4

If to merge the circuits that implement functions $\overset{=}{F}_3, \overset{>}{F}_3, \overset{<}{F}_3$, then the digital comparator to compare two 3-binary numbers will be (conditional graphic images on Fig.9.5):

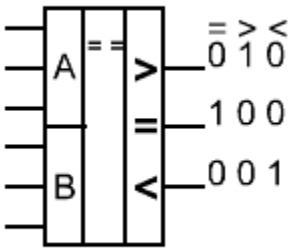


Fig. 9.5

9.3. Digital comparator based on adder

The ratio of the two numbers can be found, if from the number $A_4A_3A_2A_1$ deduct number $B_4B_3B_2B_1$ and analyze the difference $D_4D_3D_2D_1$. That is the same if to $A_4A_3A_2A_1$we add the number $B_4B_3B_2B_1$in reverse code:

$$\begin{array}{l} A_4A_3A_2A_1 \\ -\underline{B_4B_3B_2B_1} \\ D_4D_3D_2D_1 \end{array} \rightarrow \begin{array}{l} A_4A_3A_2A_1 \\ +\overline{B_4}\,\overline{B_3}\,\overline{B_2}\,\overline{B_1} \\ \hline PS_4S_3S_2S_1 \end{array}$$

The table shows the possible situations on outputs of adder and the corresponding function relationships:

$\bigcap S_i$	P_i	
1	*	$\overset{=}{F}_4$
0	**1**	$\overset{>}{F}_4 = \overline{\overset{=}{F}_4} \cdot P = \overline{\overset{=}{F}_4 + \overline{P}}$
0	**0**	$\overset{<}{F}_4 = \overline{\overset{=}{F}_4} \cdot \overline{P} = \overline{\overset{=}{F}_4 + P}$

Here $\overset{=}{F}_4 = S_4S_3S_2S_1$- function for equality of 4-bit numbers, which is a conjunction output signal of the adder.

The scheme, which realize presented in the table expressions is shown in Fig.9.6.

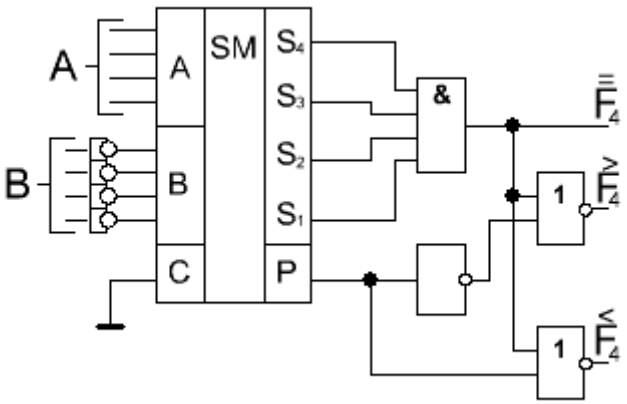


Fig. 9.6

9.4. Sectioned digital comparator

Multi-bit comparators are typically combined on the basic sections. Most often as a base can be used parallel 4-bit comparator with three outputs $\overset{>}{F}_3, \overset{=}{F}_3, \overset{<}{F}_3$. In addition to numbers A and B on its inputs get bits of the binary signals $\overset{>}{F}_3, \overset{=}{F}_3, \overset{<}{F}_3$,

which representing the result of comparison in younger tetrads of comparable numbers.

Suppose given two numbers A and B. Present them as combine of senior A_C, B_C and junior A_M, B_M tetrads:

$$A = \underbrace{A_8 A_7 A_6 A_5}_{Ac} \underbrace{A_4 A_3 A_2 A_1}_{A_M} = A_C A_M ,$$

$$B = \underbrace{B_8 B_7 B_6 B_5}_{B_C} \underbrace{B_4 B_3 B_2 B_1}_{B_M} = B_C B_M .$$

Function $\overline{\overline{F}} = (A = B)$ is the result of equal of senior and junior tetrads:

$$\overline{\overline{F}} = (A_C = B_C)(A_M = B_M) = \overline{F}_C \cdot \overline{F}_M .$$

For the functions $\overset{>}{F}$ and $\overset{<}{F}$ can take the expressions:

$$\overset{>}{F} = (A_C > B_C) + (A_C = B_C) \cdot (A_M > B_M) = \overset{>}{F}_C + \overline{F}_C \cdot \overset{>}{F}_M = \overline{\overline{\overset{>}{F}_C \cdot \overline{\overline{F}}_C \cdot \overset{>}{F}_M}} ,$$

$$\overset{<}{F} = (A_C < B_C) + (A_C = B_C) \cdot (A_M < B_M) = \overset{<}{F}_C + \overline{F}_C \cdot \overset{<}{F}_M = \overline{\overline{\overset{<}{F}_C \cdot \overline{\overline{F}}_C \cdot \overset{<}{F}_M}} .$$

Section 4-bit comparator (Fig.9.7) became as an integrated circuit (Fig.9.8-a). Sectioned comparator for multi-bit numbers can build as series circuit of 4-bit sections (Fig.9.8-б).

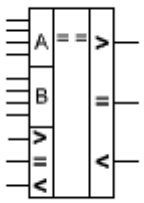


Fig. 9.7

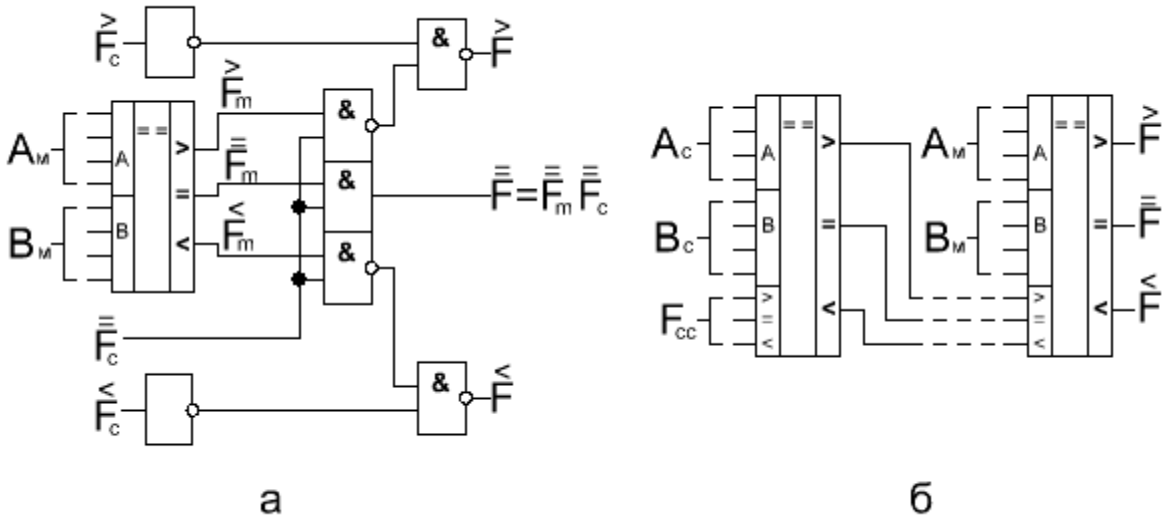


Fig. 9.8

10. Flip-flops (triggers)

Flip-flop is a regenerative triggered device with two or more stable states that are switched according to the state information inputs. In addition to information, flip-flop can have special input for synchronization and other control inputs. In our scientific and educational literature such devices often called as triggers. Therefore further we will use also this term for such class of devices.

10.1. Asynchronous RS-triggers

In asynchronous trigger states changes in consequence of the events on the information inputs. Such devices have two information inputs: R (from word “Reset”) and S (from word “Set”). Active level on input S switch RS-trigger over to state “1”, and active level on input R switch RS-trigger over to state “0”.

10.1.1. RS-trigger based on elements NOR

Circuit of the RS-trigger, based on the logic elements NOR, shown on Fig. 10.1.

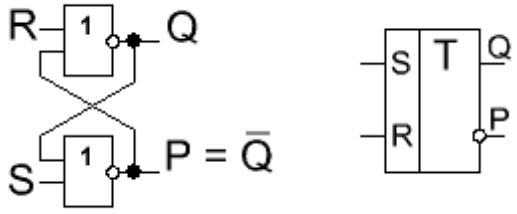


Fig. 10.1

Two-logic element NOR closed in the positive feedback loop: the output of the logic element NOR with output Q connected with one of the inputs of the other logic element, and the output of the second connected with one of the inputs of the first. Available inputs are used as informational inputs R and S of trigger. By definition, the input signal S switch over trigger in the state "1" and the input R switch over trigger in the state "0". For identification of state of trigger, take level on output Q (direct). The second output of trigger P is called inverted because normally it is the opposite state of the output Q.

The logic of the trigger can be represented as a state table:

R	***S***	***Q***	***P***	
0	**0**	Q_{n-1}	$\overline{Q}_{n-1}$	**saving mode**
0	**1**	**1**	**0**	**installation 1**
1	**0**	**0**	**1**	**installation 0**
1	**1**	**0**	**0**	**trigger gap relationships**

On the output element NOR is logical zero if at least one of the inputs given logical “1”. Directly under the scheme can determine that when R = 0, S = 0 due to feedback between any logic elements state of trigger ($Q = 1$ or $Q = 0$) is stable. This combination of control signals corresponding to the storage mode.

The combination of $R = 0$, $S = 1$ translates to trigger a logical”1” if he was in a state of logic “0”, or if it was a logical “1”, keeps it in this state. This is installation mode in "1".

The combination of $R = 1$, $S = 0$ retains state of the trigger if it was “0”, or transfers them to “0” if the trigger was before them in state “1”. This is installation mode in "0".

The combination of *R = 1, S = 1* is prohibited. With this combination trigger condition is not determined, as in this case *Q = P = 0* and output signals are not due to connection between logic elements. Therefore, this regime called as trigger gap relationships.

Boolean equation that describes the logical trigger conditions can be written with a state table or map Karnaugh:

$Q_n =$

Q_{n-1} \ R_nS_n	00	01	11	10
0	**0**	**1**	**?**	**0**
1	**1**	**1**	**?**	**0**

$= Q_{n-1} \cdot \bar{R}_n + S_n\bar{R}_n =$

$(Q_{n-1} + S_n)(S_n + \bar{R}_n)$

Installation time trigger: $t_{уст.тр.} = 2t_{зд.р.ср.}$.

10.1.2. RS-trigger based on logic elements NAND

Functional diagram of asynchronous RS-trigger-element NAND shown in Fig.10.2:

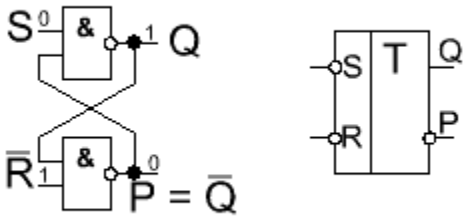


Fig. 10.2

It can be obtained directly from the circuit elements in NOR, using the principle of duality. According to this principle, any logic circuit built on elements of NOR circuit can be replaced by the elements and NOR, if this signals to the inputs and outputs replaced by their opposite meaning:

$S \to \overline{S}$, $R \to \overline{R}$, $Q \to \overline{Q}$, $\overline{Q} \to Q$.

Karnaugh map describes the state of triggers:

Q_{n-1} \ $\overline{S}\,\overline{R}$	01	11	10
0	**?**	**1**	**0**	**0**
1	**?**	**1**	**1**	**0**

$$= S_n.\overline{R}_n + Q_{n-1}\overline{R}_n$$
$$= (Q_{n-1} + S_n)(S_n + \overline{R}_n)$$

Mode of storage is provided on condition that the control signals $\overline{R} = 1,\ \overline{S} = 1$. Setting "1" is performed while changing $\overline{S}$ with logical “1” to “0”, and setting a "0" - when changes $\overline{R}$ of the logical “1” to “0”,.

Combination $\overline{R} = 0,\ \overline{S} = 0$ is prohibited. With this combination, state of trigger is not identified.

10.2. Synchronous RS-triggers

Synchronous triggers include information inputs *S* and *R* rather than input for synchronization *C*, which serves short pulses on this input determined time of transfer trigger in new state and allows the entry of new information in the trigger. All synchronous triggers are switched simultaneously.

10.2.1. RS-trigger based on logic elements NAND

Functional diagram of a synchronous *RS*-trigger with data inputs A, B and input synchronization *C* and contains an asynchronous trigger on elements 1, 2 and schema synchronization (elements 3, 4, Fig.10.3).

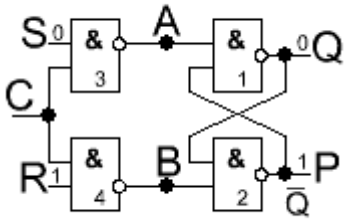


Fig.10.3

Input and output signals for asynchronous trigger ratios are determined by: $A = \overline{SC},\ B = \overline{RC},\ Q = \overline{A\overline{Q}},\ \overline{Q} = \overline{BQ}$.

Information signals on the *R* and *S* only cause the information to be recorded. While *C = 0, A = B = 1*, the trigger is in storage mode. Recording information in the trigger clock starts after the appearance of the *C = 1*. If *C = 1*, whichever is recorded in the trigger logic unit (*S = 1*) or a logical zero (*R = 1*), a trigger is set according to the "1" or "0".

State of trigger for different combinations of *R* and *S* on inputs shows the Karnaugh map:

$Q_n =$

S_nR_n / C_nQ_{n-1}	**00**	**01**	**11**	**10**
00	**0**	**0**	**0**	**0**
01	**1**	**1**	**1**	**1**
11	**1**	**0**	**?**	**1**
10	**0**	**0**	**?**	**1**

$= \bar{C}_n . Q_{n-1} + Q_{n-1} . \bar{R}_n + C_n S_n \bar{R}_n = (Q_{n-1} + C_n)(Q_{n-1} + S_n)(S_n + \bar{R}_n + \bar{C}_n)$

10.2.2. RS-trigger based on logic elements NOR

Functional diagram for a synchronous *RS*-trigger based on logic elements NOR shown in Fig.10.4.

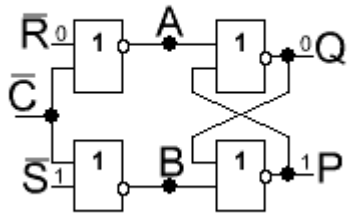


Fig.10.4

Information signals on the *R* and *S* define the information recorded. Until $\overline{C} = 1$, $Q_n = Q_{n-1}$ the trigger is in a storage mode. Recording information in the trigger begins after the appearance of the clock pulse $\overline{C} = 0$. If $\overline{C} = 0$, so depending on what is written in the trigger logic “0” ($\overline{R} = 0$) or logic “1” ($\overline{S} = 0$) trigger is set according state.

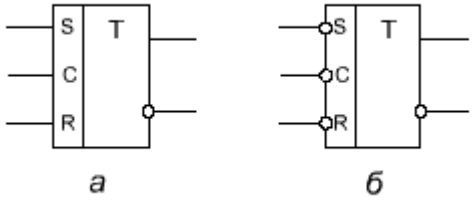
State of trigger for different combinations of *R* and *S* on inputs shows the Karnaugh map:

$Q_n =$

$\overline{C}_n Q_{n-1}$ \ $\overline{S_n}\,\overline{R_n}$	00	01	11	10
00	?	1	0	0
01	?	1	1	0
11	1	1	1	1
10	0	0	0	0

$= \overline{C}_n Q_{n-1} + Q_{n-1}\overline{R}_n + C_n S_n \overline{R}_n = (C_n + Q_{n-1})(Q_{n-1} + S_n)(\overline{C}_n + S_n + \overline{R}_n)$

A graphic representation synchronous *RS*-trigger shown in Fig.10.5 (a - on NOR, б - on NAND).



а *б*

Fig.10.5

10.3. Varieties of RS-triggers

10.3.1. R-trigger

R-trigger - this variety of RS-trigger, which reacts on the combination of input signals S = *R = 1* with transfer to "0".

Transfer of R-trigger described accordance to map Karnaugh with equation:

$Q_n =$

$C_n Q_{n-1}$ \ $S_n R_n$	00	01	11	10
00	0	0	0	0
01	1	1	1	1
11	1	0	0	1
10	0	0	0	1

$= \overline{C}_n Q_{n-1} + Q_{n-1}\overline{R}_n + C_n S_n \overline{R}_n$

$= (Q_{n-1} + C_n)(\overline{C}_n + R_n)(Q_{n-1} + S_n)$

111

The circuit, which implements this equation in basis of logic elements NAND, shown on Fig.10.6.

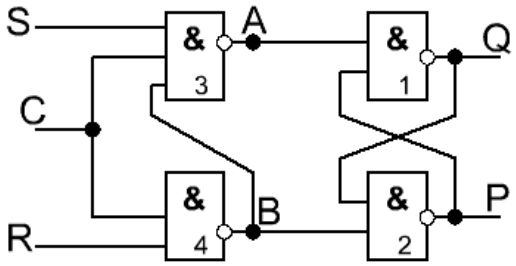


Fig.10.6

Through communication input logic element 3 of 4 with simultaneous release of the managing action $C = S = R = 1$ output 4, which is set $B = 0$, blocking other inputs element 3 and the signal $S = 1$ trigger rejects. Therefore, the combination of $S = R = 1$ sets the trigger in the state "0".

10.3.2. S-Trigger

S-trigger is a variant of *RS*-trigger, which reacts on the combination of input signals $S = R = 1$ with transfer to "1". Transfer of *S*-trigger described accordance to map Karnaugh with equation:

$Q_n =$

C_nQ_{n-1} \ S_nR_n	**00**	**01**	**11**	**10**
00	**0**	**0**	**0**	**0**
01	**1**	**1**	**1**	**1**
11	**1**	**0**	**1**	**1**
10	**0**	**0**	**1**	**1**

$$= \bar{C}_n Q_{n-1} + Q_{n-1}\bar{R}_n + \mathrm{C_n S_n}$$

$$= (Q_{n-1} + C_n)(Q_{n-1} + S_n)(\bar{C}_n + S_n + \bar{R}_n)$$

The circuit, which implements this equation in basis of logic elements NAND, shown on Fig.10.7.

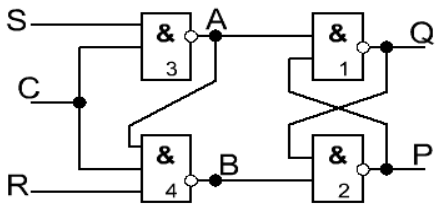


Fig.10.7

Through communication output of logic element 3 to input of logic element 4 with simultaneous release of the managing action $C = S = R = 1$ output 3, which is set $A = 0$, blocking other inputs element 4and the signal $R = 1$ trigger rejects. Therefore, the combination of $C = S = R = 1$ sets the trigger in the state "0".

10.3.3. E-trigger

E-trigger is a variant of RS-trigger, which on restricted combination of $C = S = R = 1$ does not respond, that keeps previous state: $Q_n = Q_{n-1}$.

State asynchronous E-trigger described with characteristic equation accordance to map Karnaugh:

$Q_n =$

$C_n Q_{n-1}$ \ $S_n R_n$	00	01	11	10
00	0	0	0	0
01	1	1	1	1
11	1	0	1	1
10	0	0	0	1

$$= \bar{C}_n Q_{n-1} + Q_{n-1}\bar{R}_n + S_n Q_{n-1} + C_n S_n \bar{R}_n = (Q_{n-1} + C_n)(Q_{n-1} + S_n)(Q_{n-1} + \bar{R}_n)(\bar{C}_n + S_n + \bar{R}_n)$$

The circuit, which implements such equation in the basis of logical elements NAND, shown on Fig. 10.8.

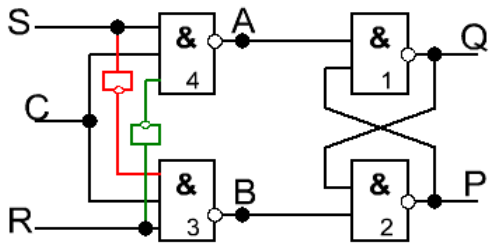


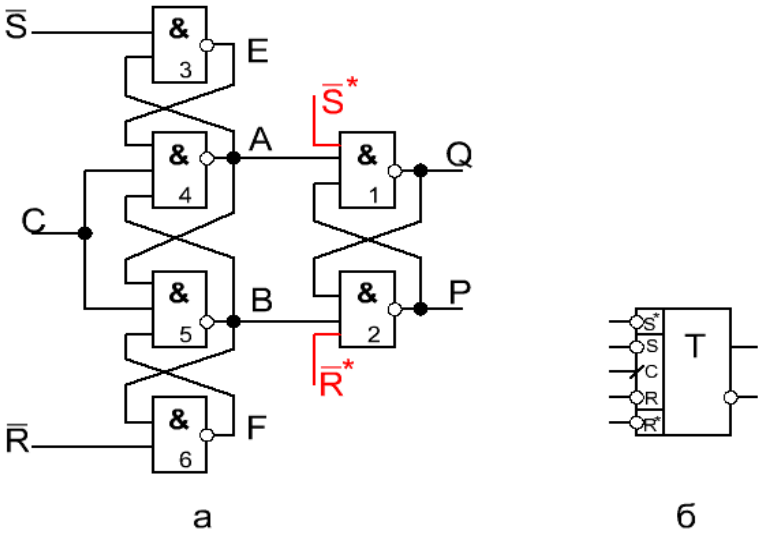
Fig.10.8

Additional inverters in case of $C = S = R = 1$ block with signals $\overline{S_n} = 0$ and $\overline{R_n} = 0$ logic elements 3 and 4, the outputs of which are supported with the level A =B = 1, which corresponds to storage mode previously recorded information.

10.4. RS-trigger “Latch” type

RS-trigger type of “Latch" consist the asynchronous trigger on logic elements 1 and 2, which is controlled by signals *A* and *B*, and the rest – are the synchronization circuit elements.

Circuit of *RS*-trigger type of “Latch" is shown on Fig.10.9-a. Besides the main trigger on logic elements 1 and 2 circuit includes triggers for synchronization: trigger on elements 3-4, trigger on elements 4-5 and trigger on elements 5-6. A graphic



representation of synchronous *RS*-trigger type of “Latch" shown on Fig.10.9-б.

Fig.10.9

In front-synchronized RS-triggers type of “Latch” information signals *S* and *R* can be switched at any time, but the trigger records the state corresponding to the combination of input signals *S* and *R* immediately after the corresponding positive clock front on input *C*. Usually such trigger can have inputs of asynchronous installation $\overline{S}^*$, $\overline{R}^*$.

When *C = 0* at the outputs of the elements 4, 5 we have A = B = 1, so the main trigger (on elements 1,2) is in the storage mode of the previous state. In addition, the triggers on elements 3-4 and 5-6 are set to the state corresponding to the levels at the information inputs. That is shown in the table below.

$\overline{S}_n$	$\overline{R}_n$	*C = 0*					*C = 1*					*Regime*
		A	*B*	*E*	*F*	*Qn*	*A*	*B*	*E*	*F*	*Qn*	
0	*0*	*1*	*1*	*1*	*1*	*Qn-1*	*0 (1)*	*1 (0)*	*1*	*1*	*?*	*Unspecified*
1	*0*	*1*	*1*	*0*	*1*	*Qn-1*	*1*	*0*	*0*	*1*	*0*	*Setting "0"*
0	*1*	*1*	*1*	*1*	*0*	*Qn-1*	*0*	*1*	*1*	*0*	*1*	*Setting "1"*
1	*1*	*1*	*1*	*0*	*0*	*Qn-1*	*1*	*1*	*0*	*0*	*Qn-1*	*Storage*

When switching $C = 0 \rightarrow 1$ signal synchronization circuit switch according to the table when $C = 1$. As seen from the table, the main trigger when C = 0 does not react to events on the inputs $\overline{S}, \overline{R}$ because $A = B = 1$ corresponds to storage mode. At constant $C = 1$ the main trigger is also not responsive to the input switching $\overline{S}, \overline{R}$ because level of $A = 0$ blocks the elements 3,5 or $B = 0$ blocks the elements 4,6 or $E = F = 0$ blocks the elements 4,5. Thus, the main trigger can switch only when the signal C switch from "0" to "1", that means the positive front clocks C. The triggers synchronized by clock Front, also known as “untransparent”. The functioning of the trigger described by characteristic equation (with $S^*R^* = 1$):

$$Q_n = \bar{C}_n Q_{n-1} + Q_{n-1}\bar{R}_n + C_n S_n \bar{R}_n = (C_n + Q_{n-1})(Q_{n-1} + S_n)(\bar{C}_n + S_n + \bar{R}_n)$$

Pictogram of the untransparent *RS*-triggers is shown on Fig.10.9-б. Risk synchronization input C indicate a response on the positive front.

10.5. RS-trigger MS (Master-Slave) type

This trigger (Fig.10.10-a) contains two stages: input trigger M (from “Master”, first stage) and output trigger S (from the “Slave”). The untransparency of the trigger is provided with counter-phase levels clock synchronization C and $\overline{C}$ of two stages. This at any level on the input C is one of two triggers is in storage mode, which eliminates the transmission of information from inputs S, R directly to outputs of the trigger Q, $\overline{Q}$. At C=0 trigger of a stage M is in storage mode, and the signal $\overline{C} = 1$ allows overwriting information from trigger M to stage S. When $C = 1$ the trigger M is setting in according to inputs S, R, and the stage S is in storage mode ($\overline{C} = 0$). Updating the information on the outputs and happens in 2 steps, so these triggers are called push-pull and denote by two letters T (Fig. 10.10-б).

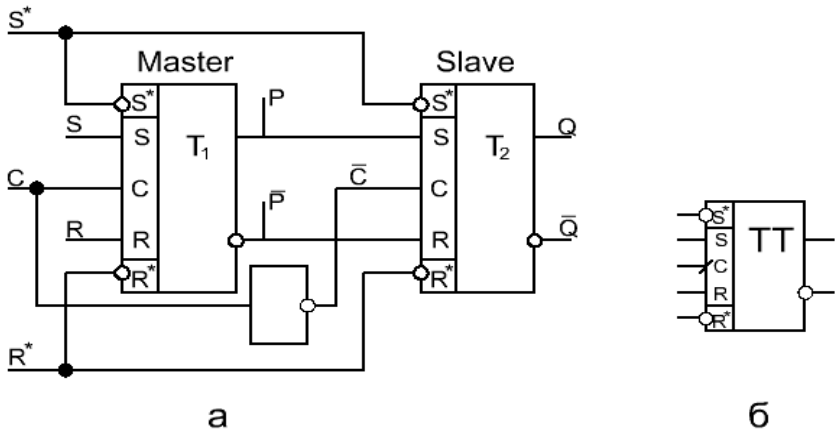


Fig.10.10

State of RS-trigger type MS represented in Karnaugh map and described by the characteristic equation that derived from it:

Q_n \ C_nQ_{n-1} \ $S_{n-1}R_{n-1}$	00	01	11	10
00	0	0	?	1
01	1	0	?	1
11	1	1	1	1
10	0	0	0	0

$$C_nQ_{n-1} + Q_{n-1}\bar{R}_{n-1} + S_{n-1}C_n\bar{R}_{n-1} = (Q_{n-1} + \bar{C}_n)(Q_{n-1} + S_{n-1})(C_n + S_{n-1} + \bar{R}_{n-1})$$

Due to the untransparency of the RS-triggers of type “Latch” and MS, it is allowed to include feedback $S = \overline{Q}$ and $R = Q$ (Fig.10.11-a). In this case only one input *C* left free, which switches the trigger to the opposite state at the front of the clock (Fig. 10.11-б). This is a T-trigger which works as a frequency divider on 2: $f_{вых} = f_{вх} / 2$.

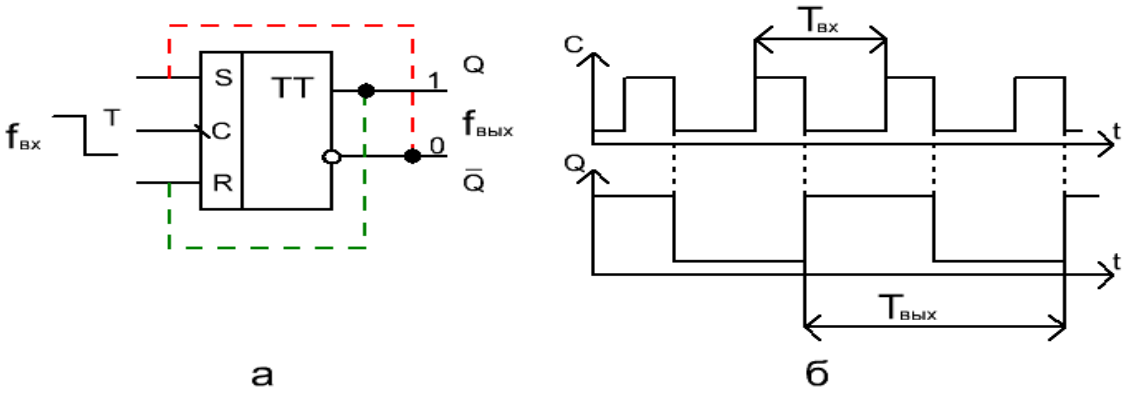


Fig.10.11

10.6. D-triggers

D-triggers include sequential devices with one information input *D* (from word Delay) and clock input *C*, which are set to a state due to the logical signal level at the input D_n = (0,1) and are paused between the clock pulses in the information storage mode ($Q_n = Q_{n-1}$).

Operation of synchronous D-trigger described with static Karnaugh map and the corresponding characteristic equation:

Q_{n-1} \ C_nD_n	00	01	11	
0	**0**	**0**	**1**	**0**
1	**1**	**1**	**1**	**0**

$Q_n =$

$$= C_n D_n + Q_{n-1}\bar{C}_n$$

$$= (Q_{n-1} + C_n)(\bar{C}_n + D_n)$$

Implementing synchronous D-trigger satisfying the resulting equation shown on

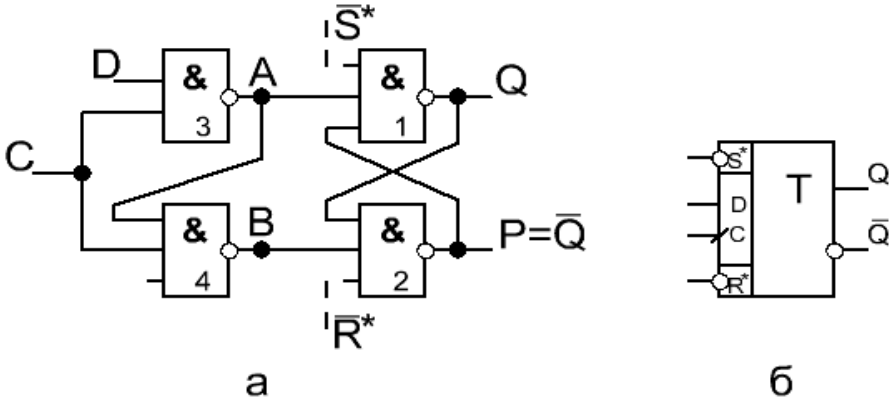


Fig.10.12-a:

Fig.10.12

If the on input of synchronization act level C = 0, which is dominant for the elements 3 and 4, their outputs set the levels A = B = 1 and do not depend on the status of the information input D. That provide the storage mode of the asynchronous trigger $Q_n = Q_{n-1}$.

If C = 1 D information input determines the state of the output element 3: $A = \overline{CD}$, which in turn determines the level inverse output element 4. When D = 0 is set to zero trigger condition: $Q_n = 0$ ($A = \overline{CD} = 1,\ B = \overline{CA} = 0$). When D = 1 trigger is set in state $Q_n = 1$. That means, that in D- trigger written information presented to the input D to the setting of synchronizing *C* = 1. Thus, information on the outputs of D-trigger appears with delay of the information on input D, due to delayed clock pulses on the information signal C and delay time switching of logic elements 1-4.

Graphic representation of such transparent D-trigger is shown on Fig.10.12-б.

10.7. D-trigger “Latch” type

D-trigger type of “Latch” that synchronized with positive front of signal C is shown in Fig.10.13-a:

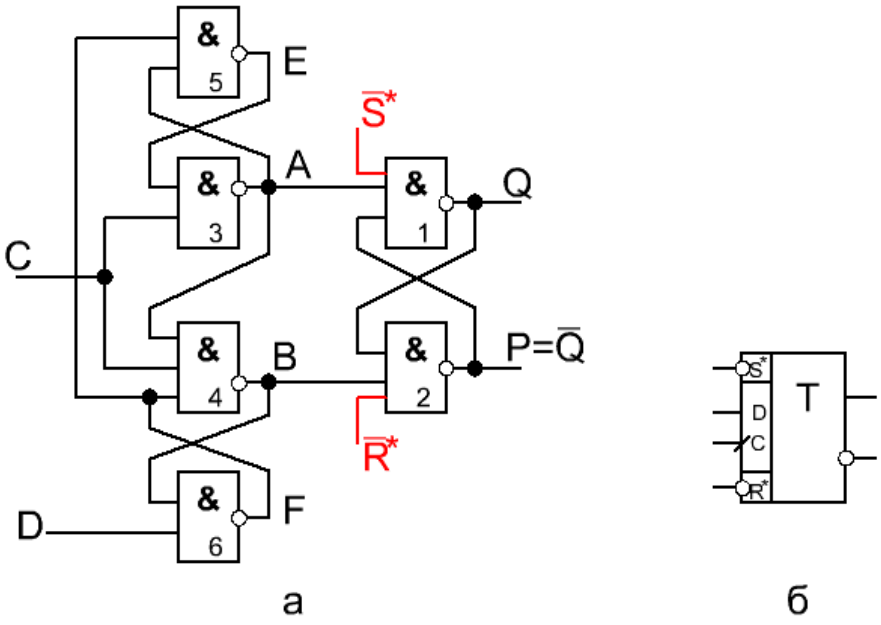


Fig.10.13

It is built on three triggers, including triggers for synchronization on logic elements NAND 3-5 and 4-6 and the basic cell synchronization circuit for storing information on logic elements NAND 1-2.

Switching output status Q, $\overline{Q}$ and of control signals *A, B, E, F* due of positive front of the impulse shows next table:

D	C = 0					C = 1					Trigger mode
	A	B	E	F	Q_n	A	B	E	F	Q_n	
0	1	1	0	1	Q_{n-1}	1	0	0	1	0	Setting "0"
1	1	1	1	0	Q_{n-1}	0	1	1	0	1	Setting "1"

As the table shows, when *C* = 0 switch of level on the input *D* affects only the logical state of the levels *E* and *F* triggers synchronization scheme: if *D* = 0, *E* = 0, *F* = 1, while *D* = 1 we have *F* = 0, *E* = 1. Therefore one of the triggers synchronization circuit is in a stable condition, while the other trigger is in mode break ties at the level of "logic 1" on both outputs.

On the positive front of the clock pulse $C = 0 \to 1$, the trigger, which was previously in the mode of breaking the trigger connections, goes into a normal stable state and at the inputs of the main trigger are formed mutually inverse logic levels. If

D = 0, then *A = 1*, B = 0 and the trigger is set to Q_n=0; if *D = 1*, then *A* = 0, *B* = 1 and the setting is Q_n=*1*.

Characteristic equation that describes a static state "latch" is similar transparent D-trigger: $Q_n = C_n D_n + Q_{n-1}\bar{C}_n = (Q_{n-1} + D_n)(C_n + D_n)$

A graphic representation of D-trigger type of “Latch” is shown in Fig.10.13-б.

In the untransparent D-trigger may be included feedback $D = \overline{Q}$ (Fig.10.14-a). This one trigger input C acts as a T-input and that is counter to mod2 and frequency divider (Fig. 10.14-б): $f_{вых} = f_{вх}/2$.

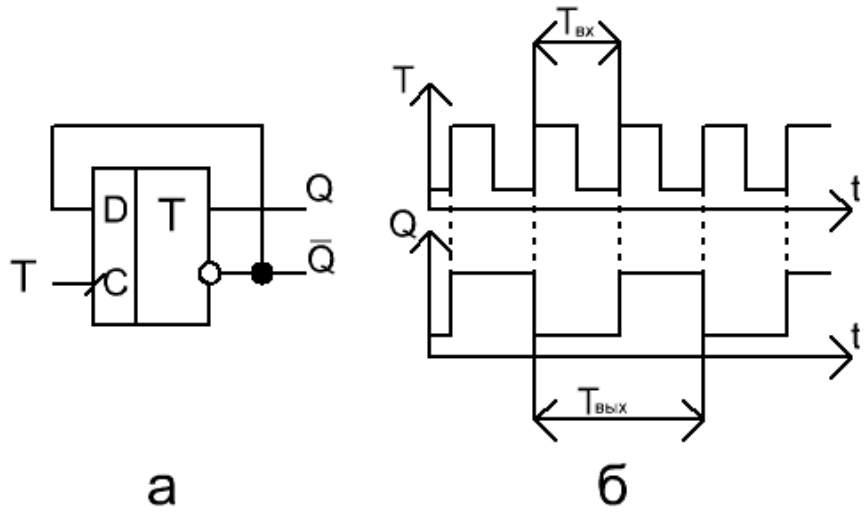


Fig.10.14

10.8. D-trigger MS (Master-Slave) type

MS-type push-pull structures are also used to eliminate cross-control in D-triggers. Two-stroke D-trigger is built because on two D-triggers that are synchronized with anti-phase levels (Fig. 10.15-a).

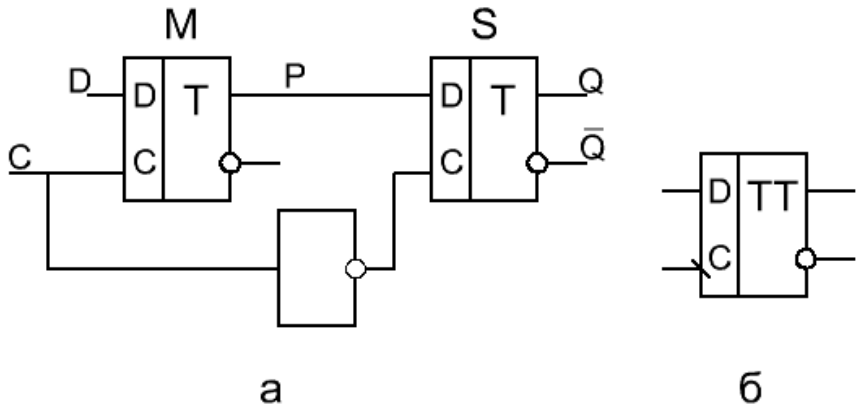


Fig.10.15

A graphic representation of D-trigger type of MS is shown on Fig.10.15-б.

Through to the synchronization with the anti-phase clock C and $\overline{C}$ the recording of new information in the triggers of the stages *M* and *S* is fundamentally separated in time, which eliminates the transfer of information from the input *D* to the outputs.

If $C = 0$ trigger of stage *M* is in storage mode, and the output trigger (stage *S*) level $\overline{C} = 1$ is allowed to overwrite the contents of the stage *M* in stage *S*. Switching clocks $C = 0 \to 1$ and $C = 1 \to 0$ triggers changes the mode *M* and *S*: *M* trigger switches to record information of the door *D*, and trigger *S* - saving mode information by the previous step. In trigger *M* is possible recording mode that is not synchronized during the sync interval $C = 1$. After switch of the clock C ($C = 1 \to 0$) input *D* is locked and in the main trigger S rewritten completely steady state of stage M (Q = P).

Static operation of the trigger type D-MS described with Karnaugh map and the equation:

$Q_n =$

Q_{n-1} \ S_nD_{n-1}	00	01	11	10
0	0	1	0	0
1	0	1	1	1

$$= C_n Q_{n-1} + \bar{C}_n D_{n-1} = (Q_{n-1} + \bar{C}_n)(D_{n-1} + C_n)$$

10.9. Universal JK-trigger MS type

JK-trigger is the bistable device with two information inputs *J* (from the English "Jerk") and *K* (from the English " Kill"), which in the case of input combination *J = K = 1* switch trigger in the opposite position, and in any other combination they function as RS-trigger inputs, whose role inputs *S* and *R* inputs are performed under *J* and *K*: $J \equiv S,\ K \equiv R$.

Functional diagram JK-trigger MS type is shown in Fig.10.16-a. The principal difference between JK-trigger of two-stroke RS-trigger is to use feedback from the outputs $Q, \overline{Q}$ to the inputs of logic elements 1,2. Through feedback banned for RS-trigger combination $S = R = 1$ for JK-trigger $J = K = 1$ switch clearly to the opposite state.

In the circuit on Fig. 10.16, instead of additional inverter that generates a signal $\overline{C}$ used signals *A, B,* which blocking logic elements 3,4 when writing a new state to the stage *M* (when $A = 0$ or $B = 0$).

States of such triggers describe Karnaugh map and the characteristic equation:

$Q_n =$

C_nQ_{n-1} \ $J_{n-1}K_{n-1}$	00	01	11	10
00	0	0	1	1
01	1	0	0	1
11	1	1	1	1
10	0	0	0	0

$= C_nQ_{n-1} + Q_{n-1}\overline{K_{n-1}} + J_{n-1}\overline{C_n}\,\overline{Q_{n-1}} =$

$(\overline{C_n} + Q_{n-1})(J_{n-1} + Q_{n-1})(C_n + \overline{K_{n-1}} + \overline{Q_{n-1}})$

Two-stroke JK-trigger (Fig.10.16-) is not critical to the duration of controlling and timing signals.

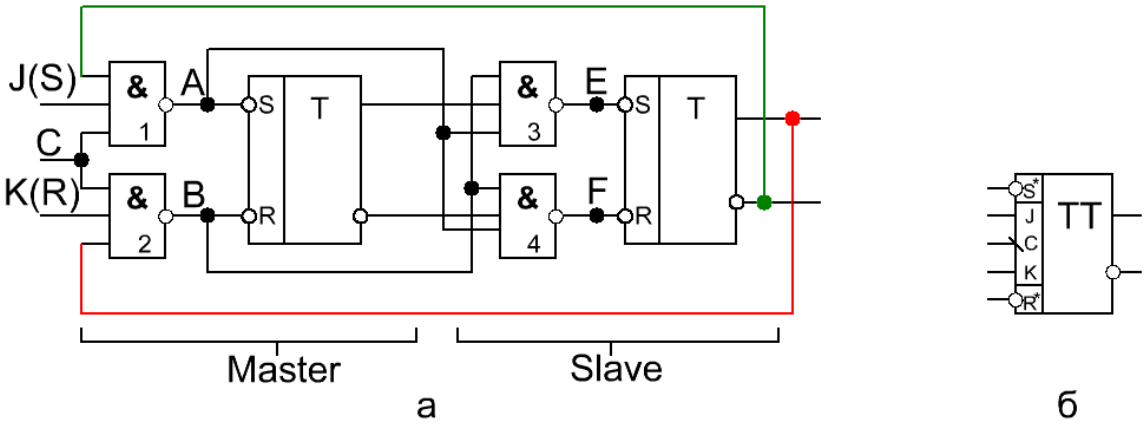


Fig.10.16

Fig.10.17-a shows how to the use JK-trigger as D-trigger, and Fig.10.17-б shows how to the use JK-trigger as T-trigger.

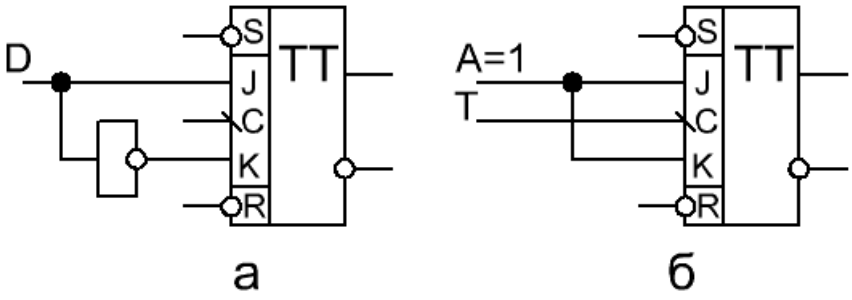


Fig.10.17

Additional inverter on input allows JK-trigger as a simultaneous two-stroke D-trigger. If J and K inputs connect to a constant level of A = 1, we get T-push-pull trigger (Fig.10.17-b). This is the universality of JK-flip-flops, which are widely used in the construction of parallel and serial registers, calculating various devices, adders etc.

10.10. JK-trigger "Latch" type

The circuit of JK-trigger of type "Latch" is shown on Fig.10.18-a. The main trigger built on logic elements 1,2. The scheme of synchronization consist the triggers on logic elements 3-5, 3-4 and 4-6. The logic elements 7,8 with the information inputs respectively J and K connected feedback signals from the outputs Q and $\overline{Q}$ so that when $J = K = 1$ provided switching of the trigger to the opposite state.

Modes trigger condition and intermediate logical variables A, B, E, F when switching clocks C = 0> 1 are shown in the table below:

Jn	*Kn*	Q_{n-1}	*C = 0*					*C = 1*					Regime
			A	*B*	*E*	*F*	Q_n	*A*	*B*	*E*	*F*	Q_n	
0	0	0	1	1	0	0	0	1	1	0	0	0	Storage "0"
0	1	0	1	1	0	0	0	1	1	0	0	0	Storage "0"
1	0	0	1	1	1	0	0	0	1	1	0	1	Setting "1"
1	1	0	1	1	1	0	0	0	1	1	0	1	Setting "1"
0	0	1	1	1	0	0	1	1	1	0	0	1	Storage of "1"
0	1	1	1	1	0	1	1	1	0	0	1	0	Setting "0"
1	0	1	1	1	0	0	1	1	1	0	0	1	Storage of "1"
1	1	1	1	1	0	1	1	1	0	0	1	0	Setting "0"

J	*K*	*C = 0*					*C = 1*					Regime
		A	*B*	*E*	*F*	Q_n	*A*	*B*	*E*	*F*	Q_n	
0	0	1	1	0	0	Q_{n-1}	1	1	0	0	Q_{n-1}	Storage
0	1	1	1	0	Q_{n-1}	Q_{n-1}	1	$\overline{Q_{n-1}}$	0	Q_{n-1}	0	$Q_n = 0$
1	0	1	1	$\overline{Q_{n-1}}$	0	Q_{n-1}	Q_{n-1}	1	$\overline{Q_{n-1}}$	0	1	$Q_n = 1$
1	1	1	1	$\overline{Q_{n-1}}$	Q_{n-1}	Q_{n-1}	Q_{n-1}	$\overline{Q_{n-1}}$	$\overline{Q_{n-1}}$	Q_{n-1}	Q_{n-1}	$Q_n = \overline{Q_{n-1}}$

As can be seen from the table of states of the trigger, at $C = 0$ the variables *A, B,* which control the state of the main trigger on logic elements 1-2, retain the value $A = B = 1$, which corresponds to the storage mode, since for the logical elements NAND dominant is level "0". In this case, the variables *E* and *F* take the values determined by the input signals *J, K,* depending on the state of the trigger Q_{n-1} before switching the level at the clock input.

Switching the clock signal C causes the transition of the triggers of the timing circuit on logic elements 3-5 and 4-6 in a stable state and the corresponding installation (or storage of the previous state Q_{n-1}) of the main trigger on logic elements 1-2.

JK-trigger can change state only when the transfer clock signals $C = 0 \to 1$, that is, its positive front. At constant C =1 or C = 0 JK-trigger does not respond to information inputs J and K. At C = 0 stored $A = B = 1$, and at $C = 1$ levels $E = F = 0$ block the inputs of the trigger on logic elements 3, 4, or $A = 0$ blocks logic elements 4, 5 or $B = 0$ blocks logic elements 3,6. This ensures the opacity of the "latch" and only works on the positive front. The JK-trigger may have asynchronous control inputs R^*, S^* for pre-installation.

States of JK-trigger (when $R^* = S^* = 1$) describes the Karnaugh map and the characteristic equation:

$Q_n =$

C_nQ_{n-1} \ J_nK_n	00	01	11	10
00	0	0	0	0
01	1	1	1	1
11	1	0	0	1
10	0	0	1	1

$$= \overline{C_n} Q_{n-1} + Q_{n-1}\overline{K_n} + J_n C_n \overline{Q_{n-1}} =$$
$$(C_n + Q_{n-1})(J_n + Q_{n-1})(\overline{C_n} + \overline{K_n} + \overline{Q_{n-1}})$$

Pictogram of such circuit is shown in Fig.10.18-б.

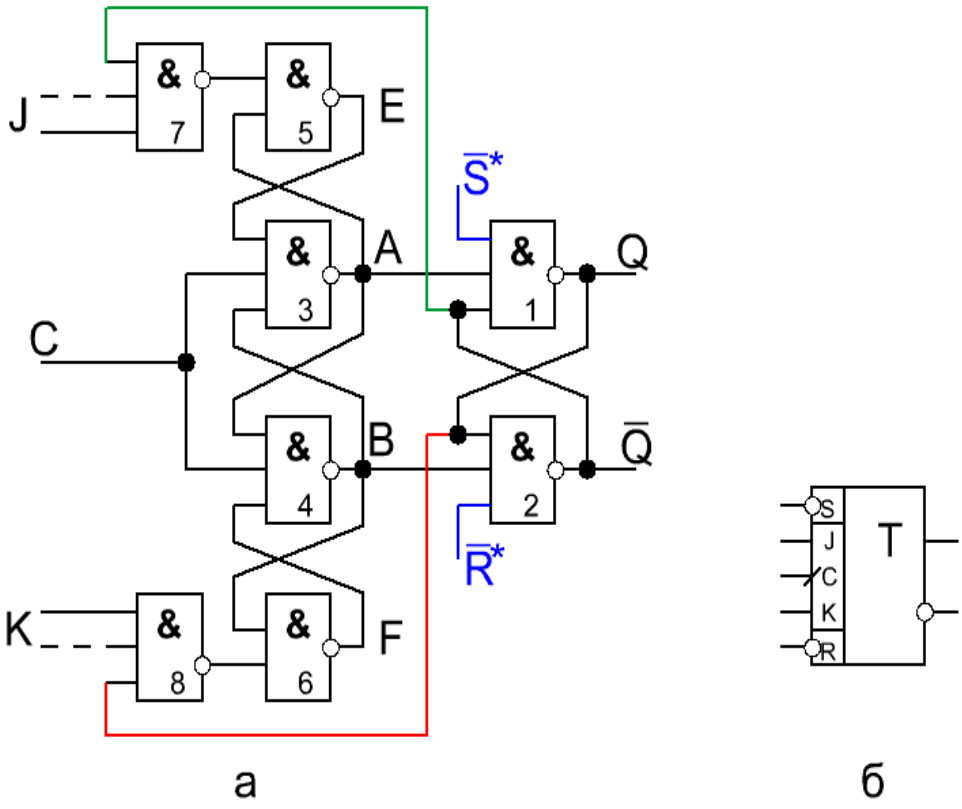
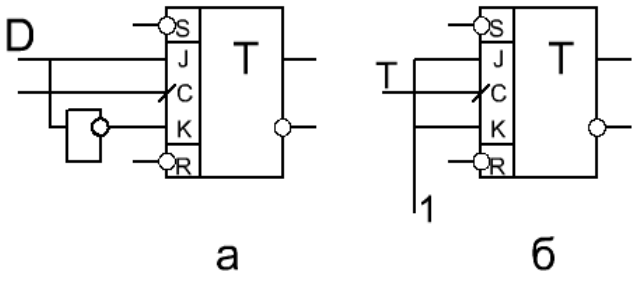


Fig.10.18

Figure 10.19 shows how to enable the JK-trigger as a D-trigger (Fig.10.19-a) with one information input *D* and as a T-trigger (Fig.10.19-б) as a single-digit



counter.

Fig.10.19

11. Registers

Registers - are devices for receiving, storing, simple transformation and transmission of multi-codes. In simple transformations implied decimal numbers to shift specified number of digits and convert serial binary code in parallel and parallel to serial. The basic elements of the registers are triggers that are complemented combinational logic elements for various connections between bits of the register and to manage the reception and transmission of operands. The main functional using of the registers is memory for multi binary numbers.

Depending on how the reception and transmission of binary information is distinguished parallel, serial, ring registers and registers in the code of Johnson. Technical parameters registers determined by the parameters of the basic functional unit of the trigger and the number of operands.

In serial registers input / output information realized through one entrance and one exit with successively shift of number. Because serial registers called shift register. For single cycle, information entered or displayed, shifted by one digit to the right or left. Shift registers that implement the command management information offset to the right or left, called reversible.

Offset number sold between neighboring states overwriting register triggers shift in direction. Thus, each bit register simultaneously receives information from the previous level and transmits the information to the next. To avoid the phenomenon of racing these processes should be separated in time. This is achieved by the inclusion of elements delays link between discharges or using triggers stroke. Parallel registers are the main functional elements for building operational storage devices.

Serial-parallel registers have one information input for sequentially entering a number in shift mode and output valves for issuing an n-bit number in parallel. Such registers convert the sequential code to parallel. These registers perform convert sequential code into parallel.

In parallel-serial registers code information is entered in parallel in one clock cycle after clock input valves and are displayed sequentially on one level in each clock interval. Thus the transformation operation is implemented parallel to serial code.

Universal registers combine the capabilities of the above types of registers and, in addition, provide a shutdown mode inputs and outputs (third logical state) register of common information bus switch of places the inputs and outputs of the register and thus switching functions of receiving / sending information to general information bus.

Technical parameters registers determined by the parameters of the basic functional unit of the trigger and the number of operands.

11.1. Parallel registers

Usually in parallel registers commonly used simple asynchronous RS-triggers and synchronous RS- and D-triggers. On Fig.11.1, 11.2, 11.3 are variants of parallel registers, different type of triggers and composition of input / output information tires. Register-based asynchronous RS-flops (Fig.11.1) before entering the next n-bit number from inputs $X_1,...,X_n$ requires prior reset all flip-flops in the zero state. Reset signal is held $R = 0$. Entering information happens in case when there is a signal $A = 1$, $R = 1$. If on some i the entrance is $X_j = 1$ then $S_i = \overline{X_i A} = 0$ and given a trigger (with inverted control) switches to state "1". If on the input $X_j = 0$ then $S_i = \overline{X_i A} = 1$ and such trigger saves the state "0". Output data from the register realized when occurs signal $B = 1$, which defines the output status $Y_k = \overline{\overline{Q_k B}}$. If B = 0, all outputs are set at 'logic 1', while $B = 1$ we have $Y_k = Q_k$. The main disadvantage of such register is the need for pre-treatment register, therefore the update information need two cycles.

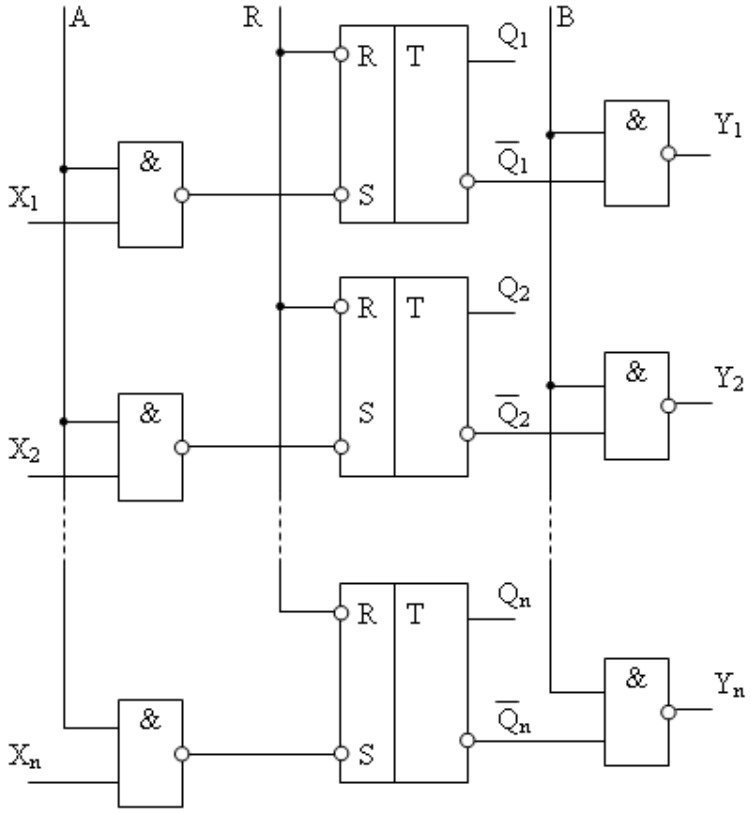


Fig.11.1

The register 0n Fig.11.2-a is also based on asynchronous RS-flops pre-treatment is not necessary, because the update information in it is the setting triggers a state of "1" and "0" in one clock cycle. To do this, the input of the register requires twice as many logical elements and communication lines.

The diagram on Fig.11.2-a shows a method of issuing information in forward code (if command $B_1=1$) AND / OR in reverse code (if command $B_2=1$). Asynchronous RS-triggers in combination with input logic (Fig. 11.1 and Fig. 11.2-a) essentially form variants of synchronous RS-triggers.

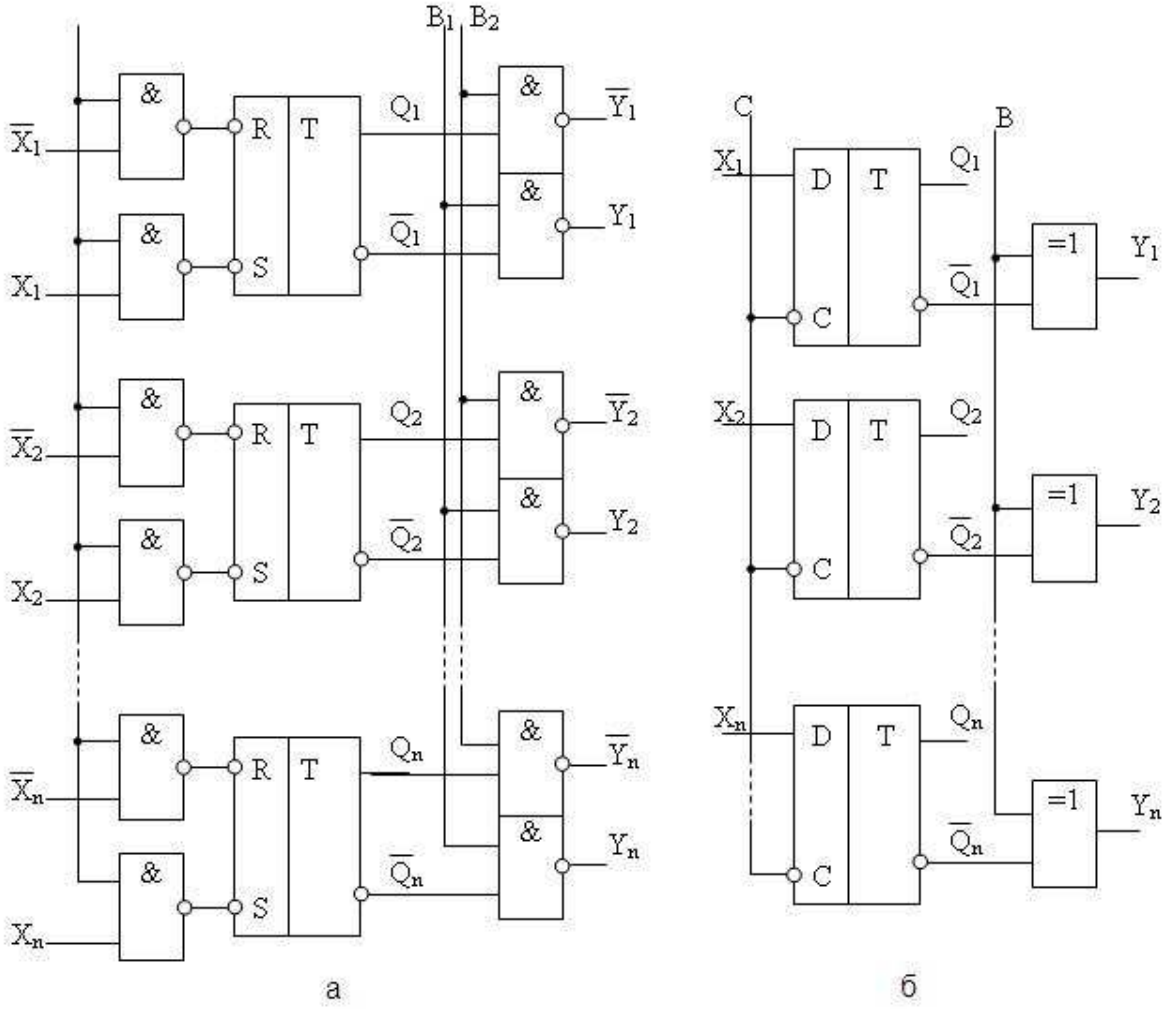


Fig.11.2

Figure 11.3 shows the scheme of a parallel register based on synchronous D-triggers. Here as inputs, the logical elements included in the *D* circuit of the triggers are used. The input of information occurs at the synchronization interval at *C=0*. As output, the logical elements AND-OR-NOT are used, which form the output signals according to the expression:

$$Y_i = \overline{\overline{B}Q_i + B\overline{Q_i}},$$

that is at $B = 1$, $Y_i = Q_i$ and information from the register issued in direct code, while at $B = 0$, $Y_i = \overline{Q_i}$ in reverse.

If the expression is identically converted to a form:

$$Y = \overline{\overline{B}Q_i + B\overline{Q_i}} = \overline{B \oplus Q_i} = B \oplus \overline{Q_i} = \overline{B} \oplus Q_i,$$

the output register circuit (Fig.11.3) can be put into logical elements EXCLUSIVE OR (Fig.11.2-b). Choose how to enter information in the register or withdrawal

usually due to performance requirements and conditions of implementation of the register in digital devices.

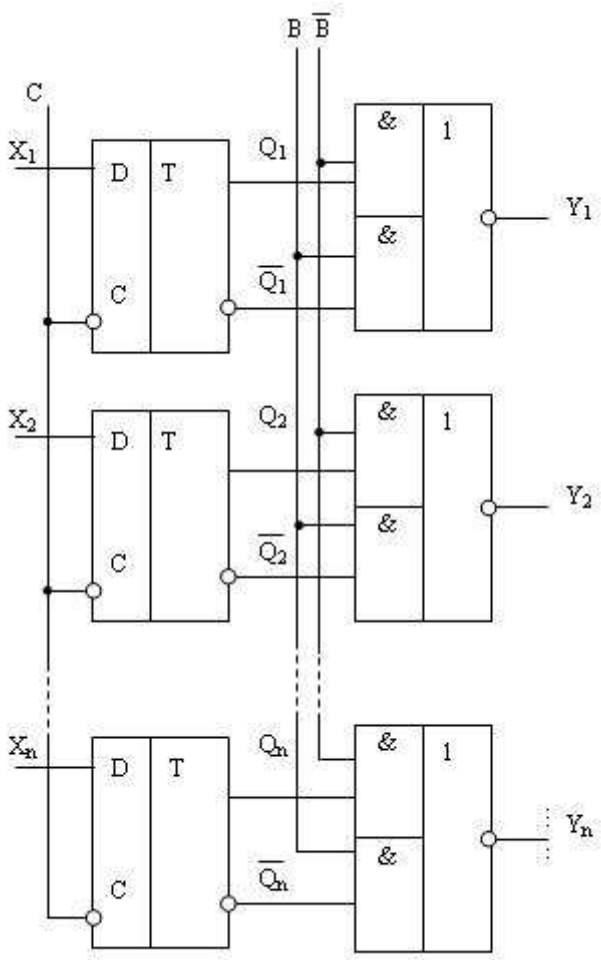


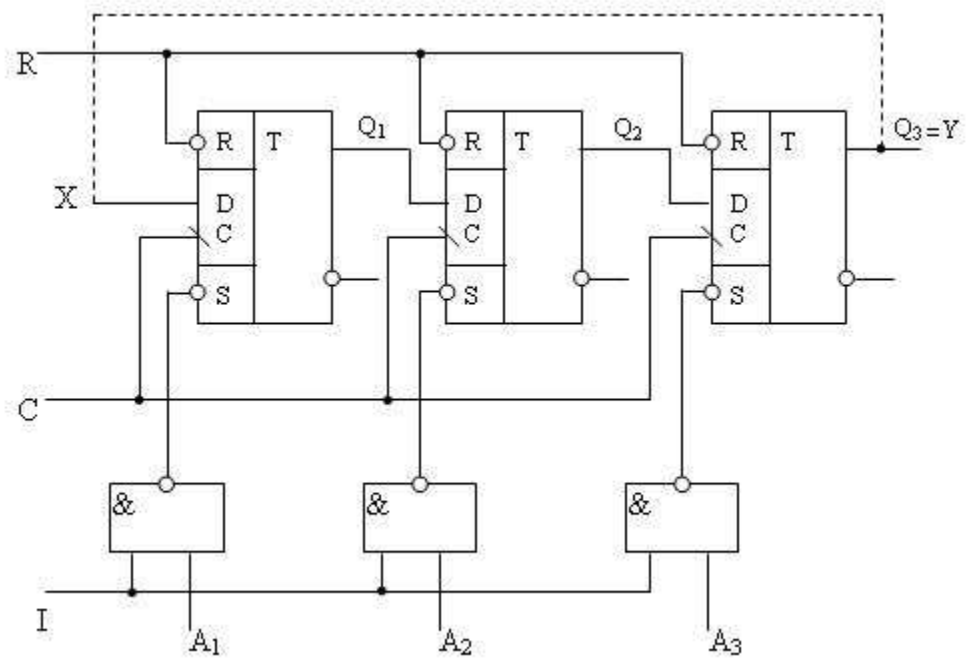
Fig.11.3

11.2. Shift register

Let us consider series-parallel and parallel-serial registers that need to perform the operation with sequential shift input and / or output. The offset of the number is realized by overwriting states between adjacent register triggers in the shift direction. Thus, each bit of the register simultaneously receives the information from the previous digit and transmits the information to the next. In order to avoid the phenomenon of racing, these processes must be separated in time. This is achieved by the inclusion of delay line elements in the communication between the digits or the use of two-stroke triggers. In integrated circuits, static shift registers are built mainly on two-stroke D- and JK-triggers.

When unidirectional shift enough information to realize direct links between inputs and outputs previous next MS-trigger (Fig.11.4, 11.5).

In the case of D-triggers (Fig.11.4) to transfer information between bits necessary link between Q_j and D_{i+1} in the case of JK-flip-flops (Fig.11.5) double



bond: Q_i with J_{i+1} and $\overline{Q_i}$ with K_{i+1}.

Fig.11.4

In both structures, the principle of operation and parameters of these registers are similar. The input of information can occur sequentially from the input *X*, with the subsequent shift of the information to the right one digit for each clock pulse *C* or in parallel from the inputs A_I on the asynchronous number recording signal to the previously cleared register (asynchronous reset of the triggers to the state "0").

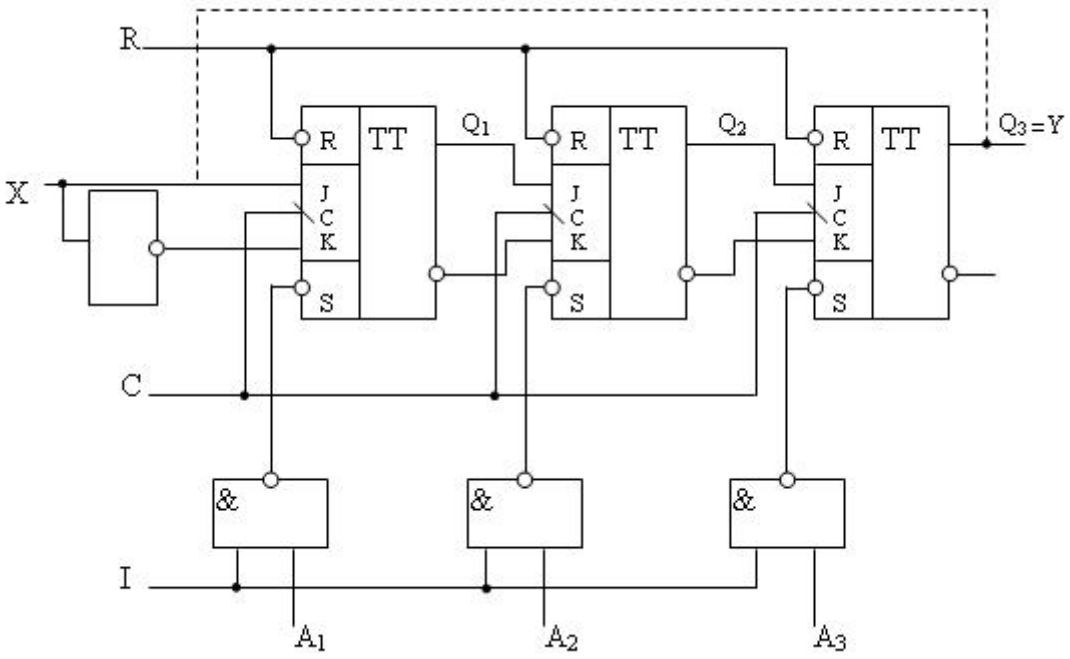


Fig.11.5

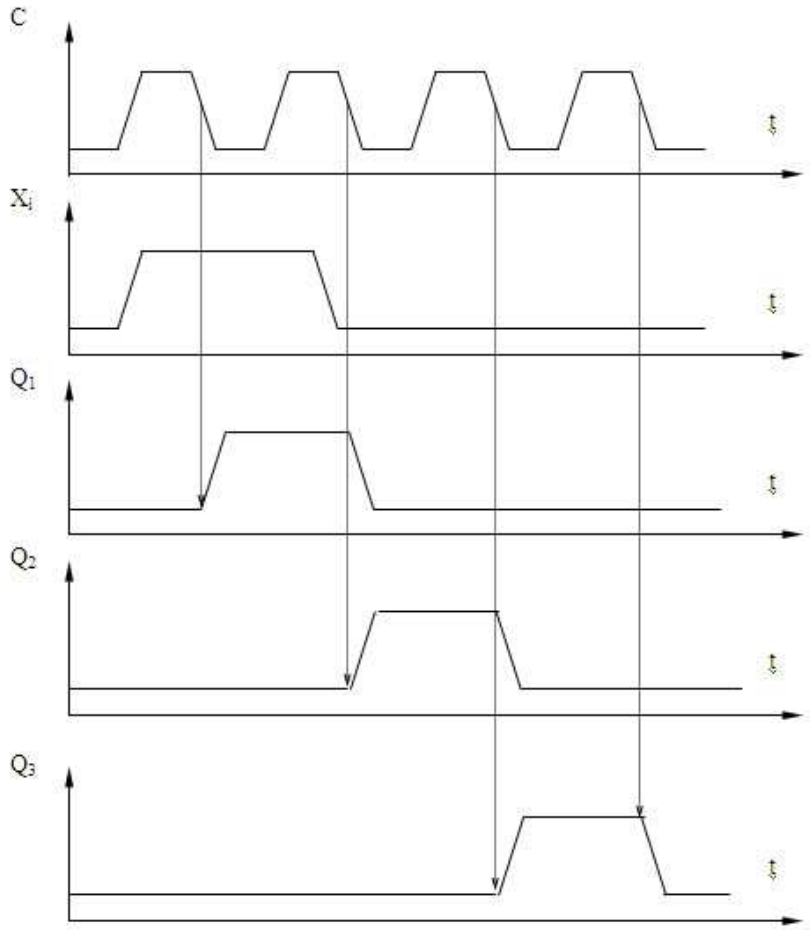
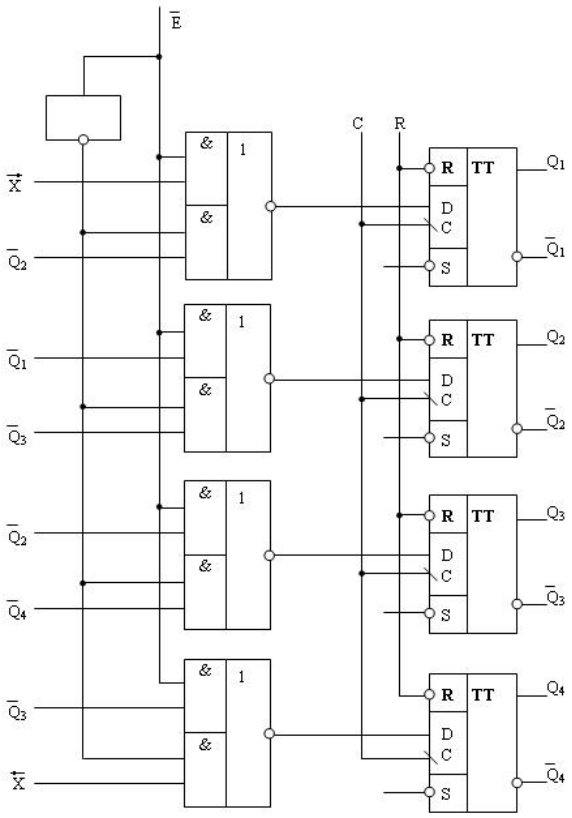


Fig.11.6

On the positive front of the clock pulse is recorded information from the inputs *D* and *X* in the triggers of the first stages of M. The output levels of the triggers remain the same (timing diagram in Fig. 11.6). On the negative front of the clock, the inputs of the D-triggers of degree M are blocked and the information recorded therein is transmitted to the flip-flops of degree *S*. The output levels of the D-flip-flops are switched. Thus, a sequential register with a shift of the number to the right (input - *X*, output - Y), serial-parallel (inputi - *X*, outputs - Q_1, Q_2, Q_3) and parallel-serial (inputs – A, output *Q3*) is implemented. In addition, when closing the output of the last digit *Q3* with a serial input *X* (dashed line) is realized annular shift register. The information in the ring register is entered by a parallel code from the inputs and then circulates in a closed ring under the action of clock C pulses.

In the reverse shift, register to enable the shift of information in both directions outputs of the triggers should be linked through logic elements of direction shift to inputs from the previous and following digits. Let the direction of shift given with logic level signal E, so that the $E = 0$ made the shift to the right: $D_i = Q_{i-1}$, while $E = 1$ made a shift to the left: $D_i = Q_{i+1}$. Then the D-trigger Q_i of reverse shift register must be controlled by signal:

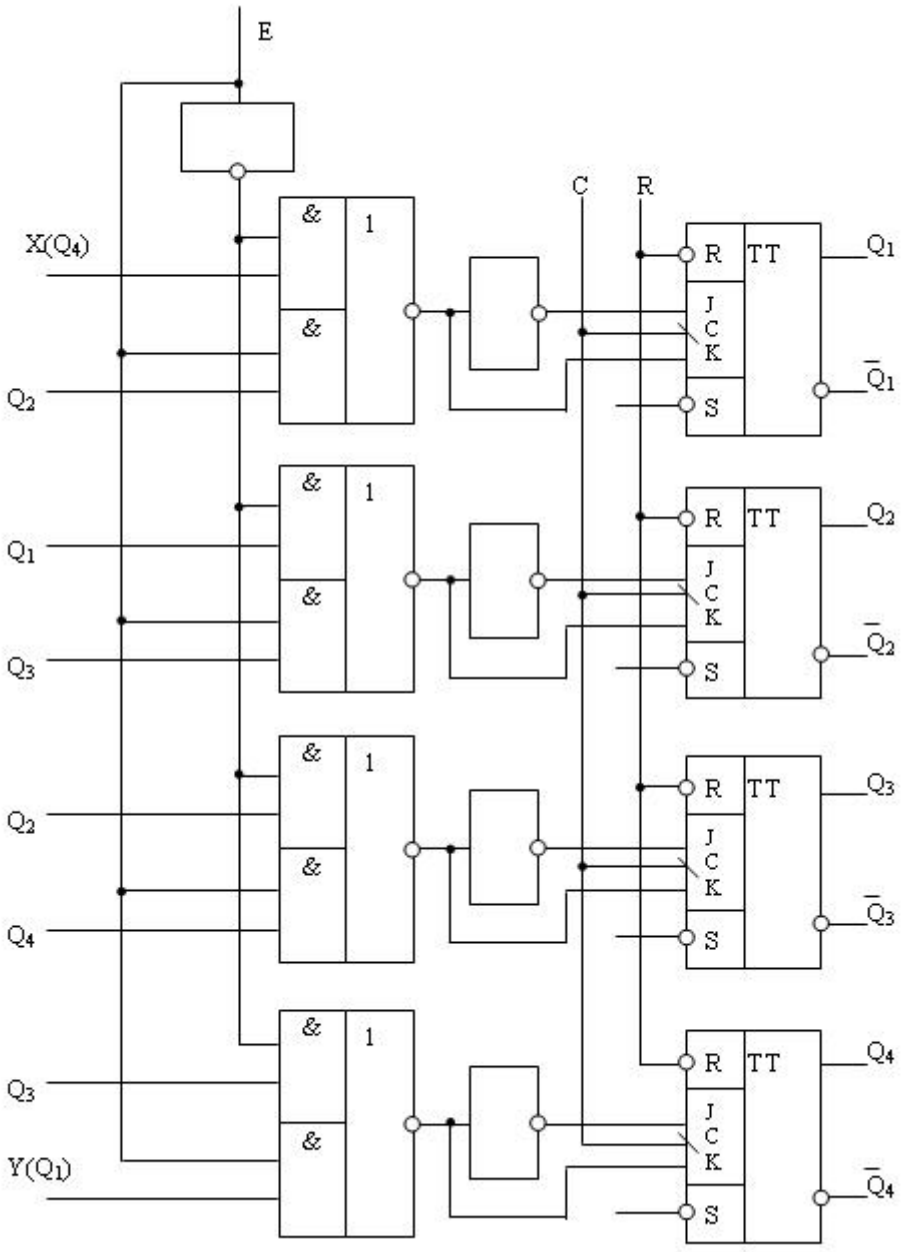


$$D_i = \overline{E}Q_{i-1} + EQ_{i+1} = \overline{\overline{E}Q_{i-1} + E\overline{Q}_{i+1}} = \overline{\overline{E}Q_{i-1}} \cdot \overline{EQ_{i+1}}.$$

Fig.11.7

Such circuit on the logical element AND-OR-NOT is showed on Fig.11.7.

Figure 11.8 shows a variant of the reversing register, built based on JK-triggers. The signal at the inputs J_i is determined similarly *Di*, and at the inputs K_i



always $K_i = \overline{j_i}$, due to inverters in the input circuits.

Fig.11.8

12. Counters (CT)

Counters are called sequential digital devices designed to calculate and store the number of pulses delivered at a specific time interval to its counting input. In

addition to counting input counters may also have inputs asynchronous and synchronous setting of initial states. Addition, subtraction, and reversible counters are distinguished by the nature of state changes. According to the method of organizing transfers between the bits, they can be divided into counters with serial, though, parallel and combined transfer.

The main technical parameters of the counters are the system of calculation, the conversion factor and the performance.

12.1. Asynchronous binary counters

In asynchronous counters, there is no total synchronization for the stages and the transition of the digits to the new states takes place consecutively stage by stage, starting from the input, which receives the counting impulses.

The asynchronous binary counter can be made in the form of a chain of T-triggers, for each of which the counting impulse is formed by the trigger of the previous (lower) stage (Fig. 12.1).

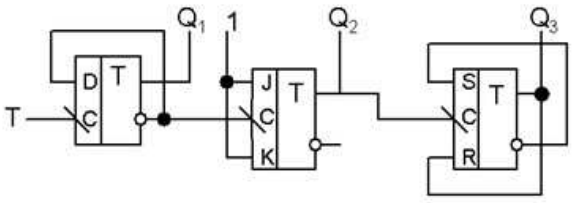


Fig. 12.1

Installation time of n-bit counter in new state:

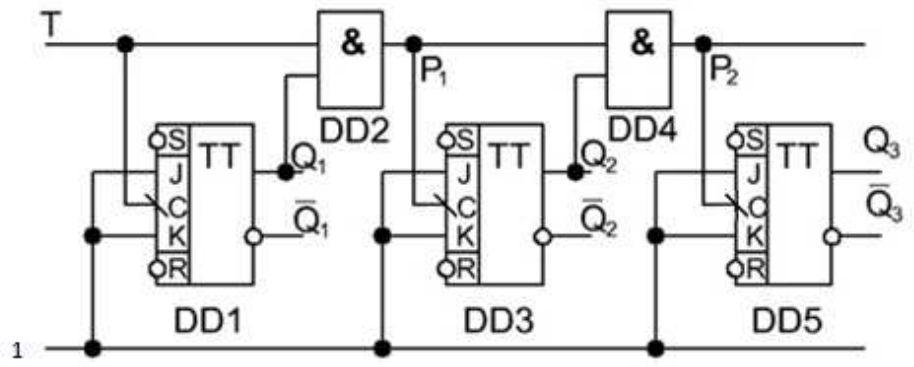
$$t_{уст.СТ} \le nt_{уст.Т.}$$

where $t_{уст.Т.}$ - time of installation of the trigger of the digits of the counter.

The main advantage of a serial counter is the low cost of circuits and the minimum of electrical connections, which simplifies the wiring of communication lines and increases the noise immunity of the circuit. The main drawback is the low performance, which is lower, the greater the coefficient $K_{сч} = 2^n$, i.e. the greater the number of bits n.

One way to increase the speed of asynchronous meters is to organize transfers between stages through additional logic elements (Fig. 12.2). Control signal A determines the mode of operation of this counter:

A = 0 - storage mode,



A = 1 - account mode.

Fig. 12.2

If the first trigger of the *DD1* counter (Fig. 12.2) is in the state "1", then the next counting impulse *T* drops it to the state "0" on the negative front. When *A* = 1 before switching the output $Q_1 = 1$, the trigger *DD1* the counting impulse T through the valve *DD2* comes in the form of a transfer pulse *P1* to the input of the second stage and the valve DD4, and if $Q_2 = 1$, then the counting impulse passes further through the valve *DD4*, etc. . The counting pulse T goes through the valves, to the second input of which comes $Q_i = 0$. The triggers from the first to the (i-1)-th are set to "0" and the i-th trigger is set to "1". In the *n*-bit end-to-end counter, the installation time is determined by the delay of the counting impulse in the transfer circuits $t_{зд.р.ср}$. and the installation time $t_{уст.Т}$ of the last of the switching triggers:

$$t_{уст.max} = (n-1)\, t_{узд.р.ср\ .И} + t_{уст.Т}.$$

Then maximum account frequency:

$$f_{сч.max} = [\, t_0 + (n-1)t_{зд.р.ср.И} + t_{уст.Т}\,]^{-1}$$

will be higher than the frequency of the serial counter because the *n-1* valve AND switches faster than the *n-1* trigger.

In terms of structure, operation and other parameters, the variants of asynchronous counters are equivalent. Depending on the number of bits *n*, they realize the coefficient of $K_{сч.}=2^n$ and can be used as frequency dividers:

$$f_{вых.} = f_{сч.} / K_{сч.} \ .$$

12.2. Reversible binary counters

The asynchronous counters considered are in the class of summaries. To implement the subtraction mode in Table 12.1 it is enough to replace "0" with "1" and vice versa, which is equivalent to removing information from the inverted outputs of the triggers (Table 12.1).

Table 12.1

№	Q1	Q2	Q3	P1	P2	P3
0	0	0	0	1	1	1
1	1	0	0	0	1	1
2	0	1	0	1	0	1
3	1	1	0	0	0	1
4	0	0	1	1	1	0
5	1	0	1	0	1	0
6	0	1	1	1	0	0
7	1	1	1	0	0	0
0	0	0	0	1	1	1

If you change the designation of the outputs of the triggers (see Figs. 12.1, 12.2) to and vice versa, the subtraction counter is obtained by sequentially connecting the inverse outputs of the previous digits with the counting inputs of the next digits of the T-triggers. Shown in Fig. 12.3 T-triggers are switched by the negative edge of the input signal, that is, the signal from the inverse output of the previous trigger. As can be seen from Fig. 12.3-b, the subtraction counter is implemented in such inter-row connections. Thus, the only difference between summation and subtraction counters is the organization of the chains of transfer from the lower digits to the senior ones or the way of reading information.

Controlled account counters are called reversible. To build a reversible counter, it is necessary to include a logic circuit between the stages, which provides the connection of the counting input of the second and subsequent digits with the outputs Q_i (addition) or $\overline{Q_i}$ (subtraction) of the triggers of the previous digits.

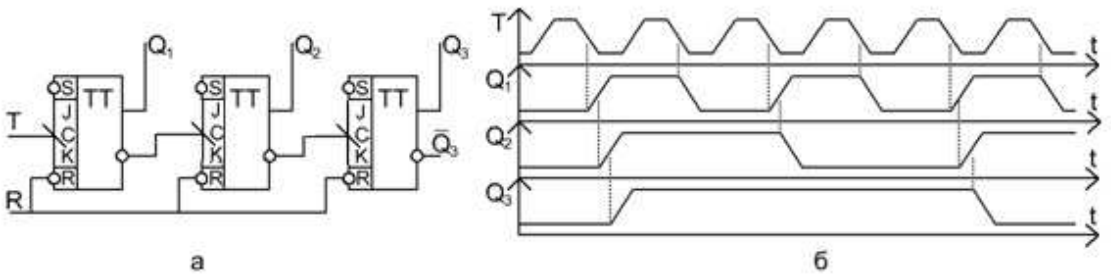


Fig. 12.3

Suppose that the direction of the account is given by the signal A such that at $A = 0$ the account with addition is fulfilled, and at $A = 1$ - with subtraction. Then the transfer signal in the i-th bit P_i is determined by the logical expression:

$$P_i = Q_i \overline{A} + \overline{Q_i} A = \overline{\overline{Q_i \overline{A}} \cdot \overline{\overline{Q_i} A}} = Q_i \oplus A \text{ .}$$

According to identical expressions, different circuit variants of transfer circuits in reversible meters can be implemented (Fig. 12.4). Reversing counter with inter-row logic of account management according to the above expression is shown in Fig. 12.4. The inclusion of additional logic elements between stages increases the time of installation of the counter and reduces the maximum rate of change of logged states.

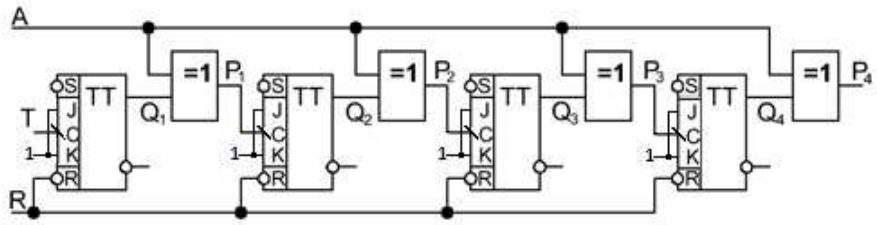


Fig. 12.4

12.3. Counters with arbitrary coefficient of account

Often, when designing digital devices, there is a need for frequency dividers for which $K_{сч}$ is any integer. If the arsenal of circuitry of the designer has the simplest details, so required $K_{сч}$ can receive due except for some states of the counter. In Fig. 12.5-а, б, в are shown the successive counters for $K_{сч}$ = 3.5,7.

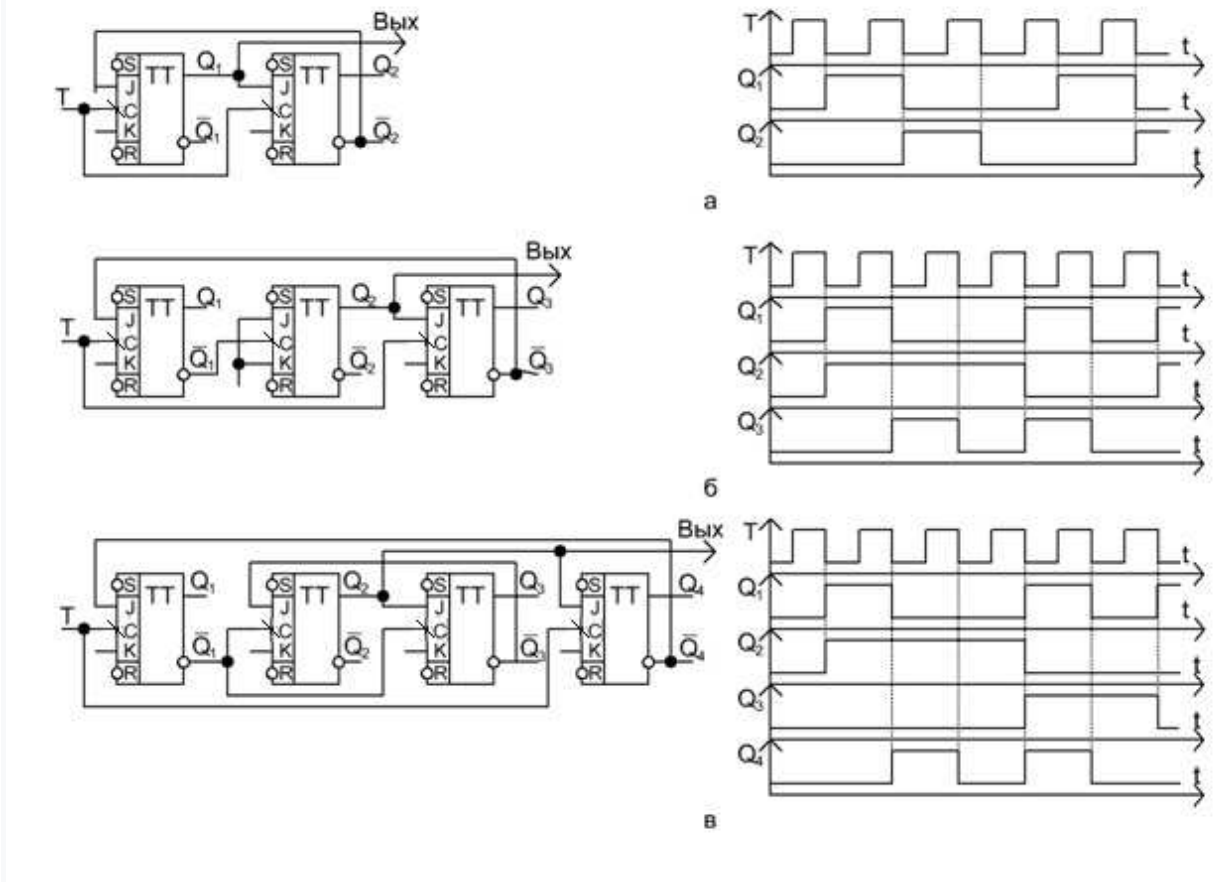


Fig. 12.5

The general principia of construction is shown in Fig. 12.5 counters with odd $K_{сч}$ is shown in Fig 12.6.

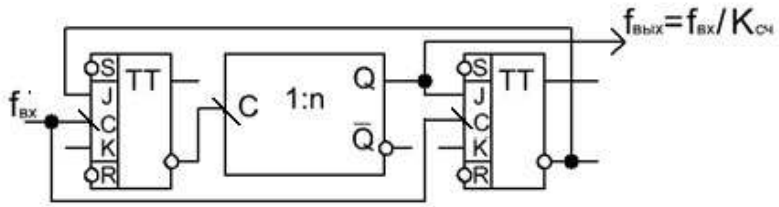


Fig. 12.6.

If a frequency divider, included between the input and output triggers, is a divider of any positive integer *n*, then this full scheme provides a frequency division on $K_{сч.}=2n+1$.

For example, the counter is a frequency divider by 3 (see Fig. 12.5-a) implemented at $n = 1$, which corresponds to the direct connection between the input *DD1* and the output *DD2* triggers. For $K_{сч} = 5$ it is necessary $n = 2$, so between the input and output triggers it is necessary to include one additional trigger - frequency

divider by 2 (Fig. 12.5-b). For the implementation of $K_{сч}$ = 7 (Fig. 12.5-в) used structure (Fig. 12.6), respectively, when *n = 3* obtained by the scheme of Fig. 12.5-a.

Shown in Fig. 12.5 sequential counters are intended mainly for use in frequency division mode without decoding their states, the change of which when using the structure (Fig. 12.6) does not correspond to the binary account.

12.4. Binary counter with controlled ratio $K_{сч}$

When constructing counter with decoding $K_{сч}$ states, it is necessary to ensure the regularity of their change according to the binary account. For their synthesis it is necessary to determine the required number of triggers *N* according to the ratio:

$$2^{N-1} \le K_{СЧ} \le 2^n .$$

In addition to N triggers, this counter should contain a logic circuit that decodes the $K_{сч}$ state and generates a reset signal of all digits to the "0" state.

If there is a need to control automatically the value of $K_{сч}$ within, then a binary counter containing N_{max} *bits*, which are determined from the condition

$$N_{\max} = [\log K_{СЧ}],$$

where N_{max} is the nearest greater integer, is constructed.

In Fig. 12.7 shows the scheme of the counter with controlled $K_{сч}$ = 1..15 for N_{max} = 4.

After $K_{сч}$ -1 pulses *B1,…., B4* logic elements *DD1,…., DD8* logic levels are set:

$$B_i = \overline{\overline{Q_i} A_i} = Q_i \overline{A_i} = 1,$$

which are fed to the inputs of the match scheme *DD9*. The following counting impulse *T = 1* through the *DD9* valve sets the RS-trigger *DD10* to a state “1” and the inverse output of the trigger causes the counter to be set to "0". Thus, due to $K_{сч}$ pulses, the counter returns to its initial state. For example, in order to realize a module 10 account, outputs A_1, A_2, A_3, A_4 must be given to code “1001”.

Uneven loading of the digits of the counter may fail - some digits will not have time to reset. To eliminate the failure in the reset scheme add RS-trigger. Because of the trigger duration the counting pulse, the input *T* provides a reliable reset of the entire counter.

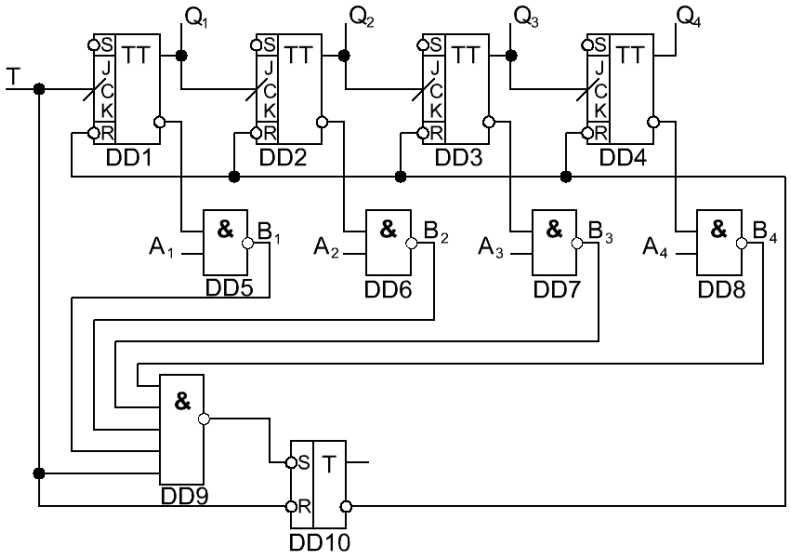


Fig. 12.7

The elimination of "superfluous" states can be performed using a digital comparator that would compare the status of the Q outputs of the counter with control code *A* (Fig. 12.8). Here, the reset signal *R* of the counter to the state "0" is determined by the expression:

$$R = (Q_1 \geq A_1)(Q_2 \geq A_2)\ldots(Q_n \geq A_n) = \bigwedge_{i=1}^{n}(Q_i \geq A_i) = \bigwedge_{i=1}^{n}\overset{\geq}{F}_i = \bigwedge_{i=1}^{n}\overline{\overset{\leq}{F}_i} = \bigwedge_{i=1}^{n}\overline{\overline{Q_i}A_i}\ .$$

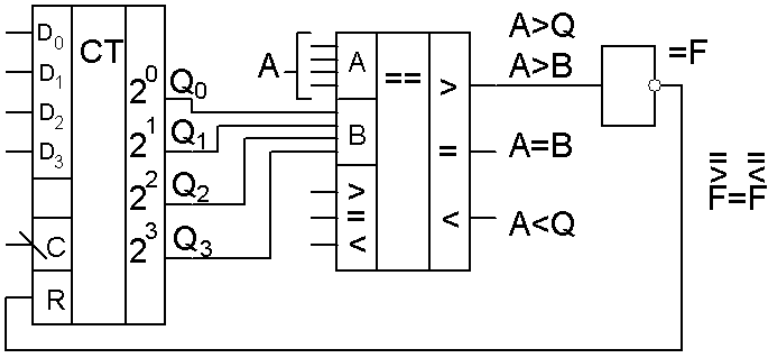


Fig. 12.8

12.5. Synchronous binary CT

Synchronous, or parallel, are the counters, in which the switching of the digits occurs simultaneously, regardless of the number of the stage of the counter. This is achieved by supplying to all triggers the clock pulses that switch all the triggers in accordance with the logic of the counter. This synchronization achieves a minimum

time of counter installation that does not exceed installation time of one trigger. Thus, the maximum frequency of changing the states of the counter ensured:

$$f_{СЧ.} = \frac{1}{t_{уст.Т.}} .$$

The scheme of the synchronous addition counter is shown in fig. 12.9. Here the transfer potential P_i is formed sequentially as logical “1” is propagated. The accumulation of the delay due to the valves of the transfer circuit causes the mutual displacement of the counting pulses T and the transfer pulses P_i. As long as the coincidence of T and P_i pulses are not disturbed by such a shift, the counter operates without interruption with the highest possible counting frequency.

The transfer from the previous category is determined by the mode of operation of counter A, as well as the conjunction Q_i:

$$P_i = AQ_1Q_2...Q_i ,$$

where if $A = 0$ - storage mode, and if $A = 1$ - counter mode.

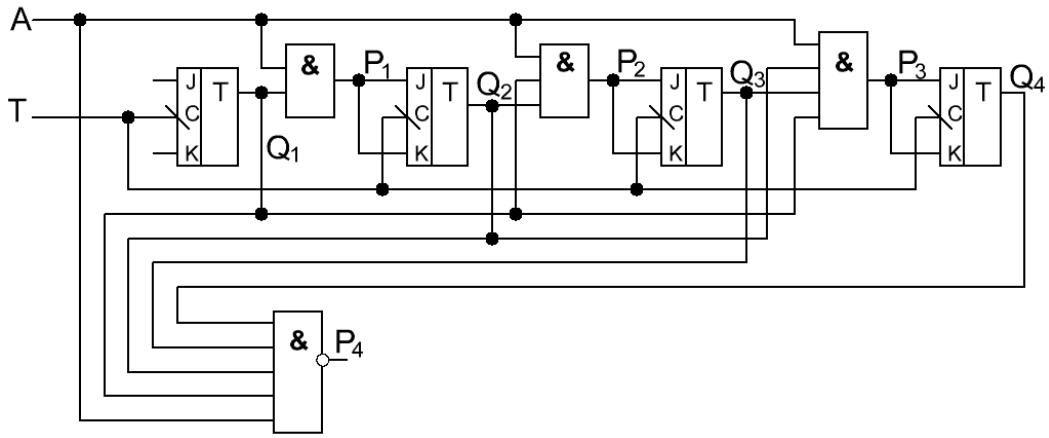


Fig. 12.9

The potentials from the outputs of the triggers are supplied simultaneously to all valves of the transfer of the higher digits, and the switching of the states of the triggers occurs synchronously. As the number of digits grows, the number of inputs of the logic elements of the transfer chain increases, so with the increase in the number of stages N, the counter circuit becomes more complicated:

$$P_i = A \bigwedge_i Q_i .$$

If the synchronous counter is built based on sections (for example, 4-bit), between them parallel circuits of parallel transfer are realized (Fig. 12.10).

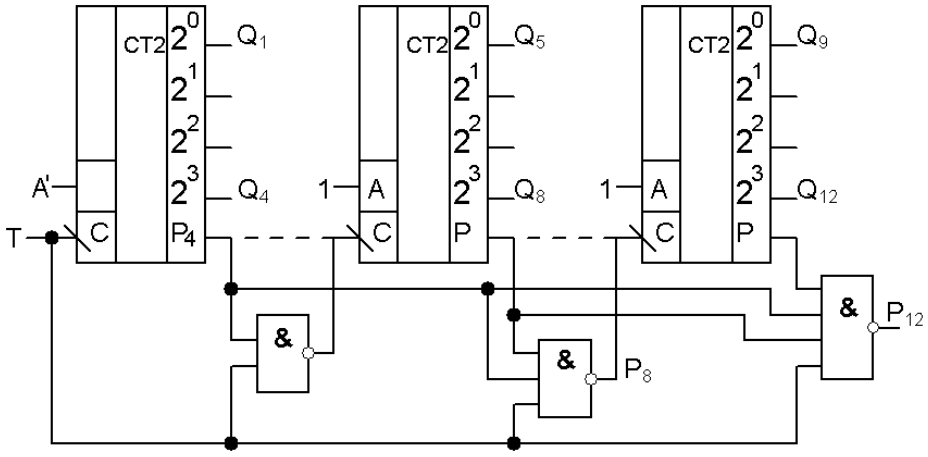


Fig. 12.10

12.6. Reversible synchronous counters

Synchronous binary subtraction counter, as well as asynchronous, is realized by the connections of the inputs of the triggers with the inverted outputs of the signals of the lower digits. As a rule, such counters should contain the inputs of the previous (synchronized) setting of the number from which the counting starts. The scheme of such a counter based on *JK*-triggers is shown in Fig. 12.11.

Signal *A* controls the state of the counter: if $A = 0$ - storage mode, and if $A = 1$ - counter mode.

Signal B controls the direction of the account: if $A = 0$ – addition mode, and if $A = 1$ – subtraction mode.

The transfer signal R_i is formed by coincidence “1” on the direct outputs of the previous triggers, and the loan signal Vi by coincidence “1” on the inverse outputs:

$$\overline{Q_i} = 1: \quad P_i = BQ_1Q_2...Q_i \; ; \quad V_i = \overline{B}\,\overline{Q_1}\,\overline{Q_2}...\overline{Q_i} \; .$$

The synchronous reverse counter can be built based on sections. Fig.12.12 shows the scheme of synchronous reverse counter with serial connection of transfer circuits and loans. In such counter of *K* sections the time of installation of the new state is:

$$t_{уст.сч.} = t_{уст.Т.} + K \cdot t_{зд.Р(V)} \; ,$$

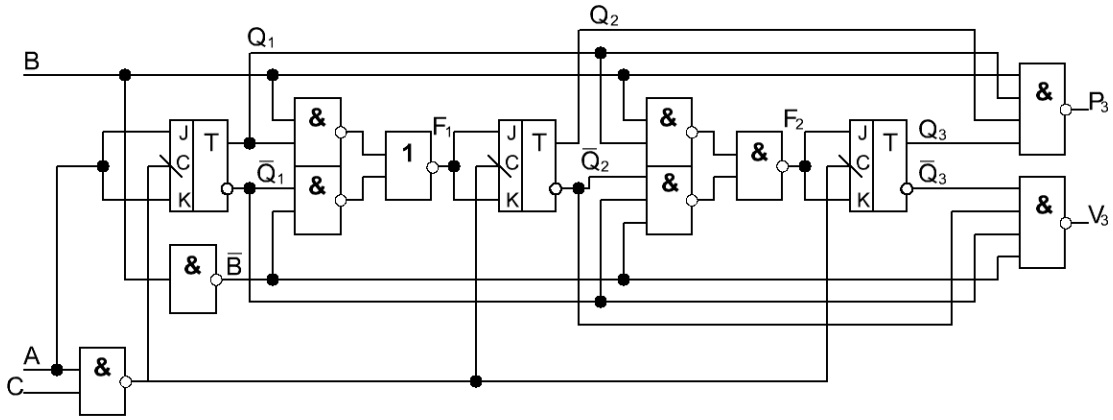


Fig. 12.11

where $t_{зд.P(V)}$ - delay propagation of the transfer signal ($t_{зд.P}$) or loan($t_{зд.V}$)3 sections. The group transfer and the loan can also be implemented in parallel, similarly to fig. 12.10. The scheme is complicated, but the installation time of the new state is minimal:

$$t_{уст.сч.} = t_{уст.T.} \cdot$$

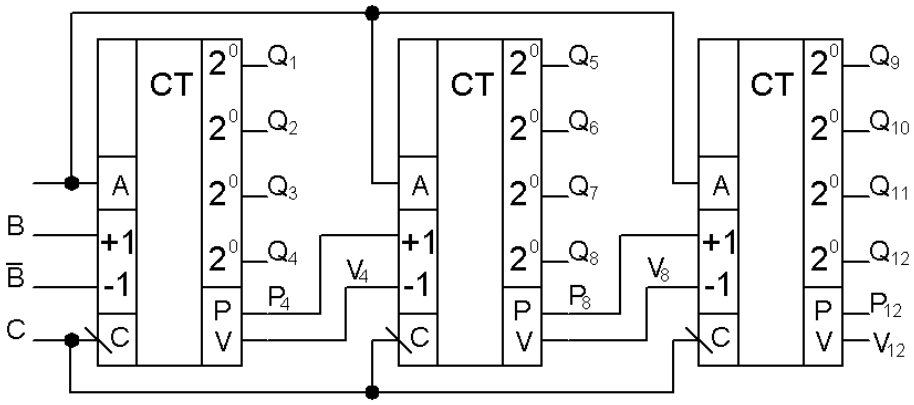


Fig.12.12

12.7. Synthesis of synchronous CTs with an arbitrary conversion table

If you want to build a synchronous counter with alternating states other than binary calculations, you need to perform a synthesis procedure that involves a certain sequence of operations. In this case, as the main components can be used any trigger synchronized front, in combination with the control circuit.

At any transitions from the previous state of the counter to the next for each type of flip-flops to the information inputs, the signals given in Table 12.2 must be reported.

Table 12.2

State	D	RS		JK		Mode
		R	S	K	J	
$0 \to 0$	0	*	0	*	0	Storage status «0»
$0 \to 1$	1	0	1	*	1	Transfer from «0» to «1»
$1 \to 0$	0	1	0	1	*	Transfer from «1» to «0»
$1 \to 1$	1	0	*	0	*	Storage status «1»

* in the table indicates that both "0" and "1" can be submitted for this transition to this input.

The basis for the synthesis control circuits of the triggers inputs *D*, *R*, *S*, *J*, and *K* is a consecutive states table of the counter, which change along the front of the clock signal *C*. The current state of the counter, through the logical controls of the inputs of the triggers of the counter prepares the transition of all digits to a new state immediately following the current one. That is, the previous state uniquely determines the status of the control inputs of the triggers of the counter to move to the next state. Then the complete set of states of the counter defines the control functions of each of the inputs, and the arguments of these functions are the states of all outputs of the triggers in the previous step of operation. Finding and implementing such control functions is the essence of the synthesis task.

Consider the procedure of synthesis of a synchronous counter with a next example. Suppose that we have to construct a 4-bit counter with the transfers according to Table 12.3.

Usually, synchronous counters are built on the same triggers. In this example, we will select different triggers to illustrate the method. Let Q_4 and Q_1 be formed by *D*-triggers, Q_2 by *RS*-trigger and Q_3 by *JK*-trigger.

To find the control function of the *D*-trigger output Q_1, we construct a Karnaugh map, whose arguments are all variables *Q1, Q2, Q3, and Q4* from the table.

Table 12.3

N	Q_4	Q_3	Q_2	Q_1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	1
3	0	0	1	0
4	0	1	1	0
5	0	1	1	1
6	0	1	0	1
7	0	1	0	0
8	1	1	0	0
9	1	1	0	1
10	1	1	1	1
11	1	1	1	0
0	0	0	0	0

The initial state of $Q_4 = Q_3 = Q_2 = Q_1 = 0$ must condition the transfer to the state of $Q_4 = Q_3 = Q_2 = 0$ and $Q_1 = 1$, as shown in Table 12.2, for this the combination $Q4 = Q3 = Q2 = Q1 = 0$ must provide at the input trigger Q_1 state $D_1 = 1$, enter in the cell of the Karnaugh map "1". Similarly, fill in all the cells of the Karnaugh map corresponding to the states of Table 12.3

D_1 =

Q_4Q_3 \ Q_2Q_1	**00**	**01**	**11**	**10**
00	**1**	**1**	**0**	**0**
01	**0**	**0**	**1**	**1**
11	**1**	**1**	**0**	**0**
10	*	*	*	*

In the Karnaugh map, * states not indicated in Table 12.3 are indicated. That is, any cells that minimize D_1 can be entered in these cells. From the Karnaugh map, we find MDNF and MCNF:

$$\text{MDNF: } D_1 = \overline{Q_3}\,\overline{Q_2} + Q_4\overline{Q_2} + \overline{Q_4}Q_3Q_2,$$

$$\text{MCNF: } D_1 = (\overline{Q_4} + \overline{Q_2})\cdot(Q_3 + \overline{Q_2})\cdot(Q_4 + \overline{Q_3} + Q_2).$$

For the *RS*-trigger that generates the signal Q_2, we find the control functions of the inputs R_2, S_2 taking into account the event table 12.2:

R_2 =

Q_4Q_3 \ Q_2Q_1	00	01	11	10
00	-	0	0	0
01	-	-	1	0
11	-	0	0	1
10	*	*	*	*

S_2 =

Q_4Q_3 \ Q_2Q_1	00	01	11	10
00	0	1	-	-
01	0	0	0	-
11	0	1	-	0
10	*	*	*	*

From the Karnaugh maps, we find:

MDNF: $R_2 = \overline{Q_4}Q_3Q_1 + Q_4Q_1;\ S_2 = Q_4Q_1 + \overline{Q_3}Q_1$,

MCNF: $R_2 = Q_3 \cdot (\overline{Q_4} + \overline{Q_1}) \cdot (Q_4 + Q_1);\ S_2 = Q_1 \cdot (Q_4 + \overline{Q_3})$.

For the *JK*-trigger that generates the Q_3 signal, we find the control functions of the inputs J_3, K_3:

K_3 =

Q_4Q_3 \ Q_2Q_1	00	01	11	10
00	-	-	-	-
01	0	0	0	0
11	0	0	0	1
10	*	*	*	*

J_3 =

Q_4Q_3 \ Q_2Q_1	00	01	11	10
00	0	0	0	1
01	-	-	-	-
11	-	-	-	-
10	*	*	*	*

From the *Karnaugh* maps, we find:

MDNF: $K_3 = Q_4 Q_2 \overline{Q_1}$; $J_3 = Q_2 \overline{Q_1}$,

MCNF: $K_3 = Q_4 Q_2 \overline{Q_1}$; $J_3 = Q_2 \overline{Q_1}$.

For the *D*-trigger that generates the Q_4 signal, we find the control function of the input D_4:

D_4 =

Q_4Q_3 \ Q_2Q_1	00	01	11	10
00	0	0	0	0
01	1	0	0	0
11	1	1	1	0
10	*	*	*	*

From the Karnaugh maps we find:

MDNF: $D_4 = Q_3 \overline{Q_2}\,\overline{Q_1}$,

MCNF: $D_4 = Q_3 \cdot (Q_4 + \overline{Q_1}) \cdot (\overline{Q_2} + Q_1)$.

We choose the basis of logical elements for this technology. If it is appropriate to use AND-NOT elements, the resulting expressions must be converted:

$$D_1 = \overline{\overline{Q_3}\,\overline{Q_2} + Q_4\overline{Q_2} + \overline{Q_4}Q_3Q_2} = \overline{\overline{Q_3}\,\overline{Q_2}} \cdot \overline{Q_4\overline{Q_2}} \cdot \overline{\overline{Q_4}Q_3Q_2};$$

$$R_2 = \overline{\overline{Q_4}Q_3Q_1 + Q_4Q_1} = \overline{\overline{Q_4}Q_3Q_1} \cdot \overline{Q_4Q_1};$$

$$S_2 = \overline{\overline{Q_4}Q_1 + \overline{Q_3}Q_1} = \overline{\overline{Q_4}Q_1} \cdot \overline{\overline{Q_3}Q_1};$$

$$K_3 = \overline{\overline{Q_4 Q_2 \overline{Q_1}}}\ ;\ J_3 = \overline{\overline{Q_2 \overline{Q_1}}}\ ;\ D_4 = \overline{\overline{Q_3 \overline{Q_2 Q_1}}}\ .$$

According to the obtained expressions for the selected types of triggers we build a scheme of synchronous counter (Fig. 12.13):

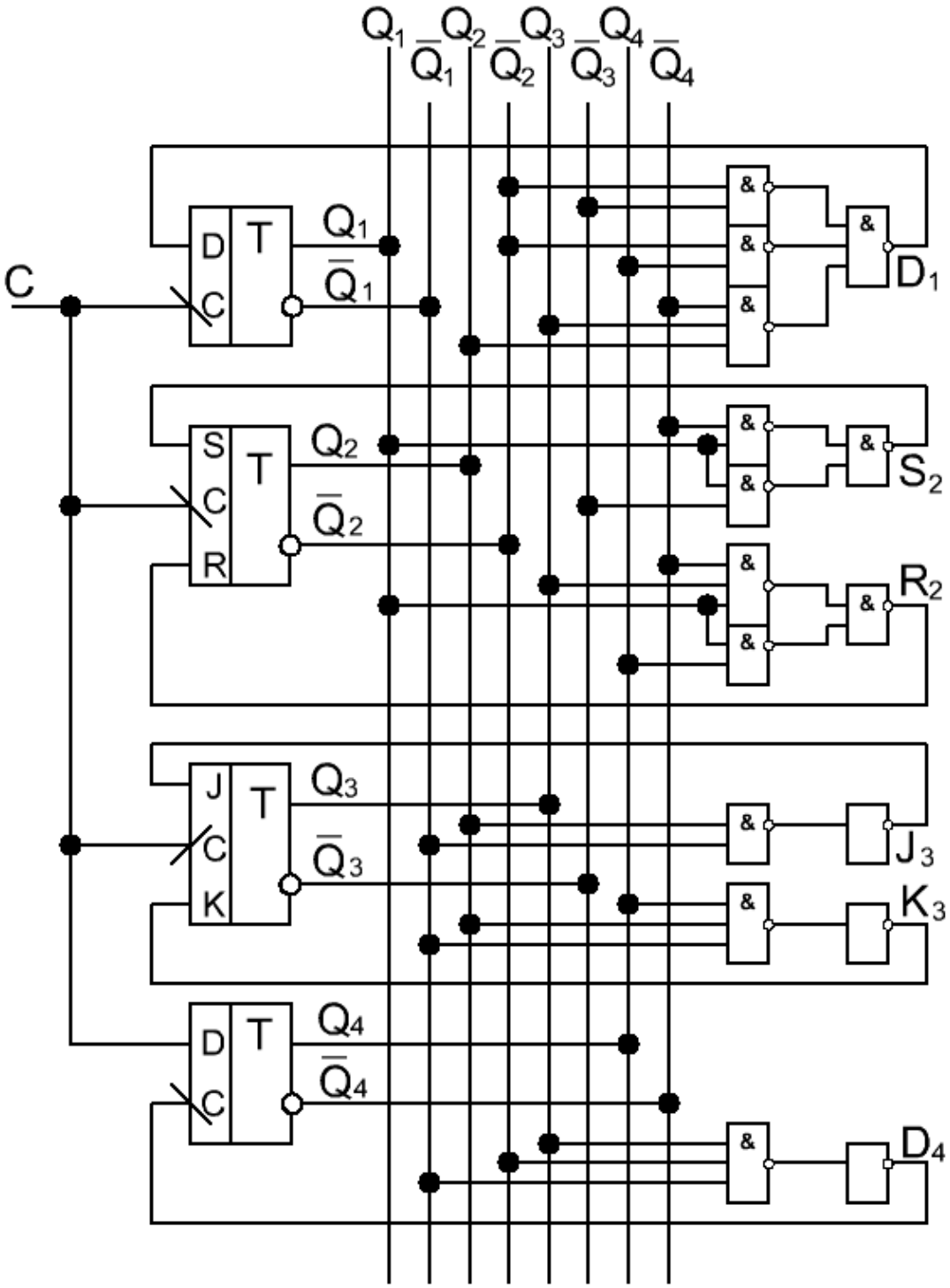


Fig. 12.13

Similarly, using the same MCNF transformations, it is possible to synthesize control circuits in other bases (NOR, AND-OR-NOT).

Thus, the synthesis of a synchronous counter with an arbitrary conversion table includes the following steps:

1. Drawing up a conversion table.
2. Choosing the type of triggers.
3. Making a Karnaugh map for each trigger information entry.
4. Finding MDNF and MCFF.
5. Convert MDNF, MCFF to the form corresponding to the selected type of logic elements.
6. Drawing up a schematic diagram of the meter.

12.8. Synchronous counter with multiplex control

Trigger control circuits can be implemented on multiplexers. The simplest counters with an arbitrary conversion table are implemented on *D*-triggers with one control input. The outputs of the triggers are connected to the address inputs A_i, and the outputs of the multiplexers control the information inputs of the *D*-triggers. The information inputs of the multiplexers provide code combinations that determine the next state of the counter.

Consider the state of the synchronous meter states defined in Table 12.4.

Table. 12.4

N	***A***	Q_1	Q_2	Q_3
0	**0**	**0**	**0**	**0**
1	**2**	**0**	**1**	**0**
2	**3**	**0**	**1**	**1**
3	**5**	**1**	**0**	**1**
4	**7**	**1**	**1**	**1**
5	**1**	**0**	**0**	**1**
6	**4**	**1**	**0**	**0**
7	**6**	**1**	**1**	**0**
8	**0**	**0**	**0**	**0**

From the state with the number "0" when $Q_1 = 0$, $Q_2 = 0$, $Q_3 = 0$, the counter must go to the state "1" when $Q_1 = 0$, $Q_2 = 1$, $Q_3 = 0$. To do this, the input of the multiplexers with the address $A_0 = Q_1 = 0$, $A_1 = Q_2 = 0$, $A_2 = Q_3 = 0$, it is necessary to

submit a combination of signals "010", which the next clock pulse will be entered in the triggers of the counter. Changing the status of the counter changes accordingly the number of information inputs of the multiplexers, from which the next combination of signals will be entered into the counter. The counter implementing the transitions according to Table 12.4 is shown in Fig. 12.14.

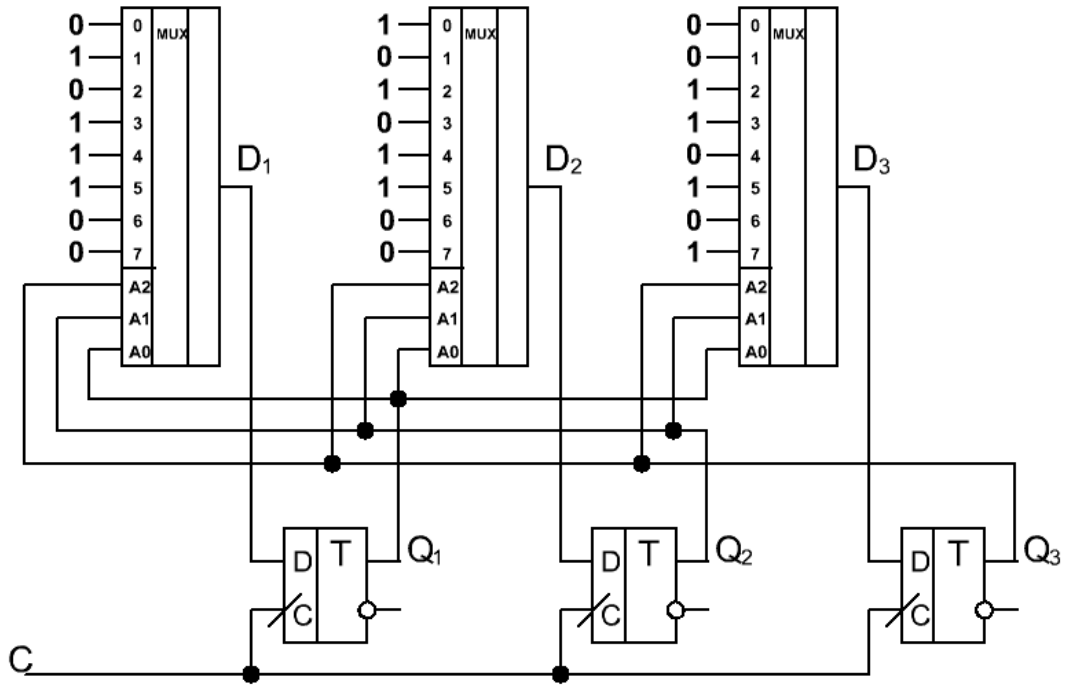


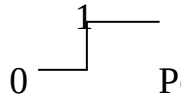
Fig.12.14

13. Impulse devices

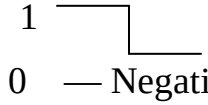
Pulse Devices - Pulse devices are devices designed to generate, generate, amplify, transmit, and transform pulses. These include pulse generators, triggers, multivibrators, counters.

13.1. Impulse front detectors

These are functional elements, designed to generate output pulse with specified parameters at the time of switching the input signal.



Positive front;



— Negative front

As parameters of the output signal is amplitude U_2 and duration t.

13.1.1. Detector of positive front (DPF)

The detector of positive front of signal U_1 shown in Fig.13.1. For each positive switching signal U_1 at the input formed output positive pulse with amplitude

$$U_2 = U^1\text{-}U^0,$$

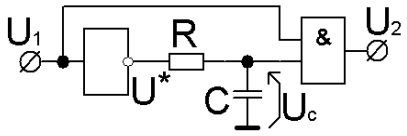


Fig. 13.1

and duration

$$t_1 = \tau^{10}\, ln\, [(U^0\text{-}U^1) \mid (U^0\text{-}U_{th.})] = C\,(R^0_{out} + R)\, ln\, [(U^0\text{-}U^1) \mid (U^0\text{-}U_{th.})]$$

where U0 - logic zero level; U^1 - logic units level, U_{th} - threshold voltage shift logic element NOT, R^0_{out} - output impedance inverter in the state "0".

13.1.2 Detector of negative front (DNF)

The detector of negative fronts of input signal U_1 shown in Fig.13.2. For each negative switching input signal U_1 at the output formed positive pulse with amplitude

$$U_2 = U^1\text{-}U^0$$

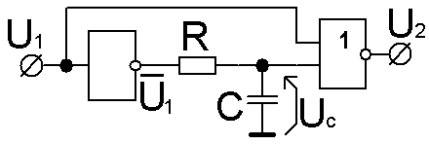


Fig.13.2

and duration:

$$t_2 = \tau^{01} ln\, [(U^1\text{-}U^0) \mid (U^1\text{-}U_{th.})] = C\,(R^1_{out} + R)\, ln\, [(U^1\text{-}U^0) \mid (U^1\text{-}U_{th.})]$$

where U0 - logic zero level; U^1 - logic units level, U_{th} - threshold voltage shift logic element NOT, R^1_{out} - output impedance inverter in the state "1".

13.1.3. Front detector (DF)

The signal edge detector U_1 is shown in Fig. 13.3. At each switch of signal U_1 at the output of the circuit, positive pulses are formed with the amplitude

$$U_2 = U^1 - U^0$$

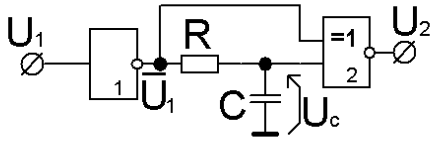


Fig.13.3

and the duration alternately t_1 and t_2.

13.2. Pulse Expander

In information systems, it is often necessary to obtain wider pulses of a certain duration from short pulses. This task is easily accomplished with the help of a pulse expander. The pulse expander (Fig. 13.4) generates a single output pulse of duration $t_{вих}$ for each input pulse of duration $t_{вх}$ of an external control signal:

$$t_{вих} = t_{вх} + \Delta t.$$

This implies that the impulse that is generated exceeds the duration of the input impulse.

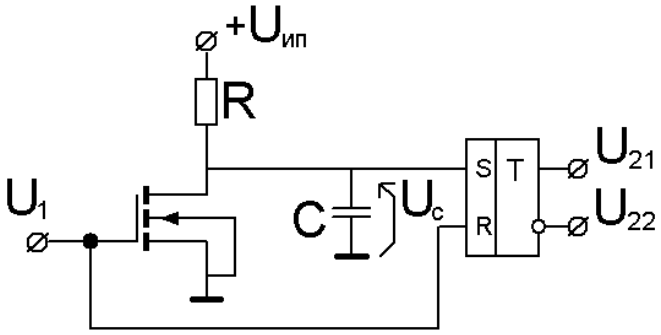


Fig.13.4

For the correct operation of the pulse expander, it is necessary that the duration of the input pulse $t_{вх}$ be sufficient to allow the capacitor to discharge completely. After the input $t_{вх}$ pulse is completed, the capacitor is charged through resistor R to the supply voltage U_{un}. In this case, as soon as the voltage reaches U_{nop} , *RS*-trigger

will switch in state “1”. In this case, the additional duration of the output pulse Δt depends on the nominal values of the installed capacitance *C* and resistor *R*. The simplified formula allows you to calculate roughly the additional pulse duration:

$$\Delta t = RC \ln [U_{un}/(U_{un} - U_{nop})],$$

where U_{un} is the supply voltage of the circuit; U_{nop} is the level of switching threshold of the RS-trigger.

13.3. Single vibrators

When working with digital devices, it is often necessary to generate impulses of a certain amplitude and duration. Special devices – single vibrators (SV), perform this function. These are trigger devices, which in response to each input pulse generate an output pulse with the desired amplitude U_2 and duration t_u. Such impulse generators can be implemented on logic elements and time-determining components *R* and *C*.

13.3.1. SV on logical elements NAND

The scheme of SV on logical elements NAND is shown in Fig. 13.5.

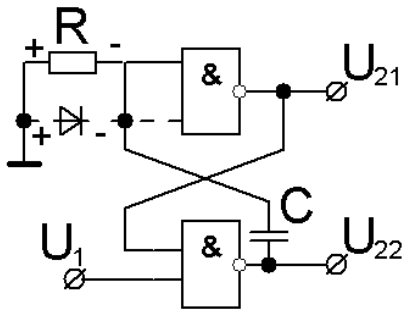


Fig. 13.5

In the scheme of the simplest single-vibrator there are two logic elements, one of them is used for its intended purpose - as a logic element NAND and the other as an inverter. For normal operation, the pulse duration of the triggering pulse must be less than the duration of the output pulse that is generated.

The pulse duration, generated by a single-vibrator, can be calculated based on the discharge condition of capacitor *C*. Until capacitor, *C* is discharged to the limit voltage U_{nop}, his voltage U_2 on input of the element NAND response to the level of logical “1” and its output is maintained at level “0”. Over time, the voltage on the capacitor *C* becomes equal to U_{nop} and at the output of the element NAND, the level

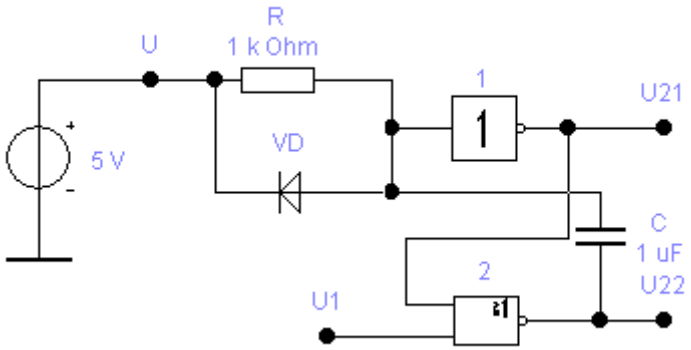
of logical unit will appear. Assuming that the voltage before the start of the discharge on the capacitor was equal to the voltage level of the logic unit U^1, then the change in voltage on capacitor C over time can be represented as an exponent with constant $\tau \approx RC$, so the duration of the output pulse t_u equals the time of discharge of the capacitor to the limit value U_{nop} is determined by the ratio:

$$t_u = RC \ln \frac{U^1}{U_{nop}}$$

13.3.2. SV on logical elements NOR

In Fig. 13.6 shows the scheme of a single-vibrator on logic elements NOT (1) and NOR (2). Alternatively, inverter 1 may be a logic element NOR with integrated inputs.

The single-vibrator, according to the scheme shown in Fig. 13.6, works as follows: in the initial state of the device at the output U_{21} of the inverter (1) there is a



low voltage level supported by the input voltage from the power supply U_{un}.

Fig.13.6

At a low level at the input *U1* of a single vibrator at the output of the logic element NOR (2) there is a high level, which makes the capacitor C practically discharged. A short positive input pulse *U1* switches the logic element NOR (2) and through the capacitor C switches the output level of inverter 1 to the "0" state. At the stage of forming the duration of the output pulse of a single vibrator, the capacitor C is charged through the resistor R and the output impedance of the logic element NOR (2) $R^0_{вых}$ with a constant exponential function $\tau_3 = C\,(R + R^0_{вых})$. The process of forming the output pulse is completed when the input voltage of the inverter 1 reaches the threshold level U_{nop}. As a result, rectangular positive impulse is formed at the output of the single-vibrator *U21* and negative impulse of is formed at the output of U_{22}. A duration t_u on both outputs is equal:

$$t_u = \tau_з \ln [(U_{un} /(U_{un} - U_{nop})] .$$

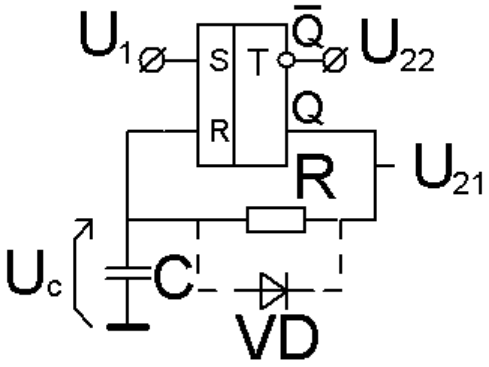
At the stage of restoration of the single-vibrator to the next starting pulse, the capacitor *C* is discharged through the output resistance R^1 of the logic element NOR (2) in the state of logic "1" and through the resistance $r_{пр}$ of the diode *VD* with constant exponent $\tau_в = C\ (R^1_{вых} + r_{pr})$. The recovery time of a single-vibrator $t_в$ is equal to:

$$t_в \approx 3\ \tau_з = 3\ C(R^1_{вих}+r_{пр}).$$

13.3.3. SV based on RS-trigger

Figure 13.7 shows the scheme of single-vibrator based on *RS*-trigger. The feedback circuit of resistor *R* and capacitor *C* between the output of trigger *Q* and the reset input of trigger *R* determines the timing of the output signal.

Consider the charging and discharging circuit of the capacitor *C* in a single vibrator. At the stage of forming the time interval t_u, the capacitor *C* is charged from "0" (more precisely, from residual voltage U^0) to the threshold voltage $U_{пор}$. Circuit



of charge: $R_{вых}$-*R*-*C*- "ground" with constant of exponent $\tau 3 = C\ (R_{вых} + R)$.

Fig.13.7

The duration of the charging process determines the duration of the output pulse t_u:

$$t_u = \tau_з\ ln\ [(U^1-U^0)/(U^1- U_{пор})].$$

In the recovery phase, the capacitor is discharged from the stop to 0 through the diode VD and the output impedance of the trigger $R_{вых}$ with constant exponential

$$\tau_{роз} = C(R+R^0_{вых}).$$

The duration of SV recovery $t_в$ can be estimated as $3\tau_{роз}$, that is:

$$t_в \approx 3\,\tau_{роз} = 3C(R+R^0_{вых}).$$

The diode is almost completely closed when the voltage on diode drops below 0.5 ... 0.6 V, and the capacitor completes the discharge with the same constant time as when forming a time interval. Thus, when the requirements for the residual voltage on the capacitor are increased, the recovery time increases.

The described single-vibrator on the *RS*-trigger has a simple structure and generates two anti-phase rectangular pulses. However, it has some disadvantages. First, the charge of the capacitor *C* occurs through the output impedance of the trigger, which causes some violation of the rectangular signal U_{21} at the direct output of the trigger. The change in $R_{вых}$ affects the duration of the generated impulse. Secondly, it is large duration time of the output pulse, the time to restore the voltage on the capacitor to its initial level.

13.3.4. SV on operational amplifier

The basis of such a single-vibrator is the Schmitt trigger (TS) on the operational amplifier (OP) (Fig.13.8). Such a trigger in this case is invertible and has two threshold levels of state switching $U_{п1}$ and $U_{п2}$, which are determined by the parameters of the positive feedback components (R_1, R_2) according to the ratios:

$$U_{n1} = U^+_0\, R_1/R_2\,, \qquad U_{n2} = -|U^-_0|\, R_1/R_2,$$

where U^+_0, $-U^-_0$ are the limit values at the TS output in two possible states, which depend on the supply voltages + Ucc1, -Ucc2. In practice, it is possible to take $U_0 \approx 0.9$ Ucc in the calculations.

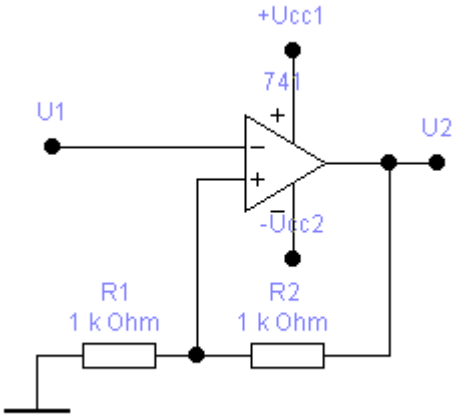


Fig.13.8

The scheme of the single-vibrator is shown in Fig. 13.9. In addition to the TS, the circuit contains components that determine the duration of the output pulse of the

SV. In this case, such components are resistor *R* and capacitor *C* in the negative feedback circuit. In addition, the SV contains a circuit for its excitation, which includes the differentiation circuit *C1-R3* and the diode *VD2*.

Prior to the arrival of the excitation pulse *U1* SV is in a stable state when the output voltage of the circuit is stable voltage $U2 = -U^-_0$. The diode VD1 is open and the capacitor C is discharged practically, since the voltage on it is equal to the voltage U0д on the open diode VD1. The positive input pulse U 1 through the diode VD2 switches the TS to a state when the output is set *at* $U2 = U^+_0$. At a high level of U^+_0 at the output, the diode VD1 closes and begins to charge the capacitor C through resistor R. The voltage on the capacitor C increases by exponential law until it reaches the threshold level Up1. Upon reaching the threshold U_{n1} TS switches to the state $U2 = -U^-_0$. This ends the formation of the output pulse of duration $t_и$:

$$t_и = RC \ln [(U^+_0 - U_{0д})/(U^+_0 - U_{п1})].$$

At the recovery stage of SV the capacitor C is discharged through the resistor R to the diode unloading voltage VD1, i.e. to $U_{0д}$. The duration of the recovery stage $t_в$ is determined by the ratio:

$$t_в = RC \ln [(|-U^-_0| - U_{n2})/((|-U^-_0| - U_{0д})].$$

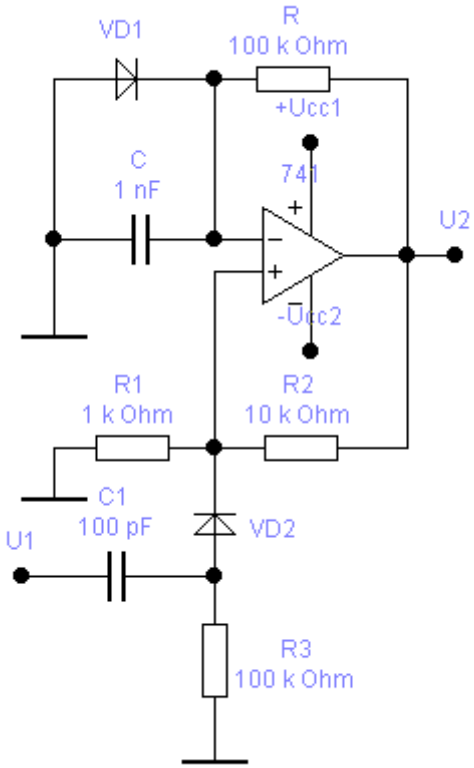


Fig.13.9

The amplitude of the positive output pulse Um is equal to:

$$U_m = U^+o + U^-o.$$

If it is necessary to obtain an SV that generates a negative output pulse in the scheme shown in Fig. 13.9, it is sufficient to change the polarity of the inclusion of diodes VD1 and VD2.

13.4. Multivibrators (MV)

The multivibrator is a relaxation generator designed to generate periodic signals (most often rectangular) with predetermined parameters: amplitude Um, frequency *f*, intermittency *Q*. MV can operate in self-oscillation mode or in the standby mode of an external start signal.

In the self-oscillation mode, the MV does not have a stable equilibrium. When operating a multivibrator in this mode, there are two alternating quasi-stable states. The state of quasi-stable characterized by a relatively slow change in currents and voltages, leading to some critical state, which creates the conditions for the jumping transition of the multivibrator from one state to another. The oscillation period depends on the scheme parameters. MV circuits can be built on the basis of bipolar transistors, unipolar transistors, operational amplifiers, logic integral elements like NOR, NAND, RS-triggers, Schmitt triggers and also on the basis of negatrons (tunnel diodes, thyristors, transistors, dynistors). Recently, MVs most often are built based on integrated circuits.

13.4.1. MV on inverters (NOT)

The scheme of MV based on logic elements NOT is shown in Fig.13.10. In addition to the inverters 1.2, the circuit contains a capacitor *C*, which provides positive feedback and, therefore, a regenerative oscillation mode. Together with the negative feedback resistor *R*, the capacitor C determines the frequency *f* and the duty cycle *Θ* of the MV output signals.

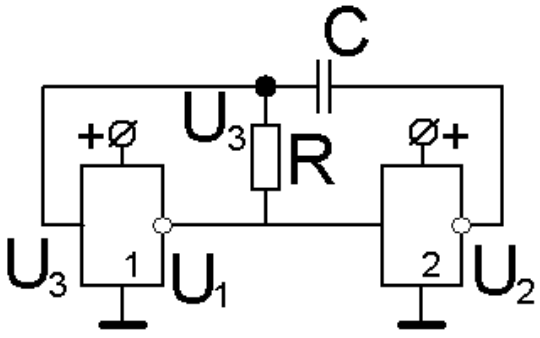


Fig. 13.10

When the power is turned on, any fluctuations or noises under the influence of positive feedback MV transfer into one of two quasi-stable states. In one of the states at the output U_1 is set low, and at the output U_2 - a high level of potential, and in the second state, on the contrary, at the output U_1 high and the output U_2 - a low level of potential. Relaxation processes of recharging the capacitor C through resistor *R*, determine the duration of the half-period T_1, *T2*, the frequency of generation *f* and the duty cycle Θ of the output pulses.

At the time interval T_1 at the input of the first element NOT is the voltage $U_3 > U_{пор}$, so its output is maintained low U^0_1, and the output of the second element is not high U^1_2. The charge current of capacitor *C* flows from the power source in the circuit $"+U_{дж.ж}" - R^1_{вих2} - C - R - R^0_{вих1} - "земля"$ and decreases exponentially with constant time:

$$\tau_1 = C(R + R^0_{вих1} + R^1_{вих2}) \approx CR,$$

where $R^0_{вых1}$ is the output impedance of inverter 1 in state "0", $R^1_{вых2}$ is the output impedance of inverter 2 in state "1".

In this case, the voltage at the input of the first element NOT fall exponentially from the initial value $U_{пор} + U^1_2$. When the voltage at the input of the first element does not reach the threshold level $U_{пор}$, the inverter of the first element goes into amplification mode, its output voltage, increasing, switches the second inverter. Further, under the influence of positive feedback, the scheme regenerative switches to the second quasi-stable state. This completes the formation of the interval T_1 of the output signal:

$$T_1 = \tau_1 \ln [(U_2^1 + U_{пор})/U_{пор}].$$

At the time interval T_2, the voltage at the input of the first element NOT is $U_3 < U_{пор}$, so the output of the first element NOT is high U_1^1, and the output of the second element NOT is low U_2^0. The charge current of the capacitor C flows in the opposite direction from the power source of the first element NOT in the circuit $"+U_{дж.ж}" - R^1_{вих1} - R - C - R^0_{вих2} - "земля"$ and creates a voltage drop on the resistor *R* sufficient to maintain at the input U_3 a voltage element in the logic region "0". As the capacitor *C* is recharged, the current through the resistor *R* decreases exponentially with constant time:

$$\tau_2 = C(R + R^1_{вих1} + R^0_{вих2}) \approx CR,$$

where $R^1_{вых1}$ is the output impedance of inverter 1 in state "1", $R^0_{вых2}$ is the output impedance of inverter 2 in state "0".

In this case, the voltage at the input of inverter 1 increases exponentially from the level $U_{пор}$ - U^1_2, asymptotically approaches the level U^1_2. At the moment of coincidence $U_3 = U_{пор}$, the circuit switches again and all processes are repeated.

The duration of the T_2 half-life, given the above formulas, is determined by the ratio:

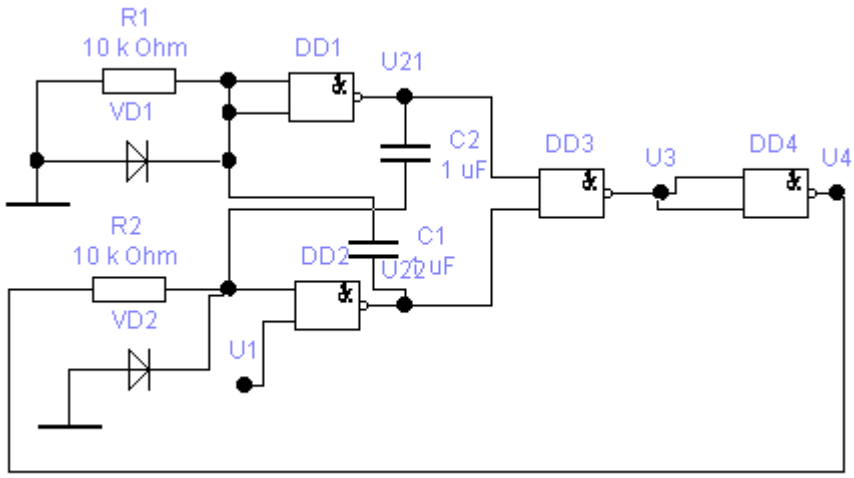
$$T_2 = \tau_2 \ln [(2U_2^1 - U_{пор})/(U_2^1 - U_{пор})].$$

The frequency of generation $f = (T1 + T2)^{-1}$ and duty cycle of output signals (ratio of output pulse duration and oscillation period):

$$\Theta_1 = (T_1+T_2)/T_1 = T/T_1, \quad \Theta_2 = (T_1+T_2)/T_2 = T/T_2.$$

The advantages of this multivibrator are the simplicity of the scheme and the stability of the frequency of generation, and a slight disadvantage is the distortion of the tops of the pulses.

13.4.2. MV on NAND with auto start



Scheme MV with auto start is shown in Fig.13.11.

Fig.13.11

This multivibrator contains two circuits *R1-C1* and *R2-C2*, which set the time parameters of the MV, that is, the frequency *f* and the duty cycle *Θ* of the output signals. The MV is built on the logic element NAND *DD1*, which is used as an inverter, and the logic elements NAND *DD2*. The *DD3* and *DD4* logic elements are designed to automatically trigger the generation mode.

In the stationary oscillation mode, anti-phase signals are set at the inputs of the *DD3* element, so a constant high level of U_3^1 is maintained at the output of the *U3* of the *DD3* element, and a low $U_4^0 \approx 0$ at the output of the *DD4* element, and the resistor *R2* is almost "grounded". In the case of failure of the oscillation signal *U1* = 0, the outputs of the elements *DD1* and *DD2* are set equal $U_{21}^1 = U_{22}^1$, therefore output *DD3* we have *U3* = 0, and the output *DD4* $U4 = U_4^1$, which through the resistor enters the input *DD2* and provides the start of the multivibrator when the trigger signal U^1_1. Thus, the generation mode is started. This allows the scheme to generate pulse packets of U^1_1 control signal duration.

External diodes provide fast discharge of capacitors *C1*, *C2* that set the time parameters of the MV: duration for the half-periods *T1* and *T2*, the frequency $f = (T1 + T2)^{-1}$ and the $\Theta 1 = (T1 + T2) / T1$.

The resistance values of the resistors *R1*, *R2* must be selected large, but subject to the limitation:

$$R_{1(2)} \le U^1_{1min} / I^0_{вх} \quad ,$$

where U^1_{1min} - the minimum voltage level for the high level;
$I^0_{вх}$ - input current of logic elements at low level at inputs DD1, DD2.

The duration of the *T1*, *T2* half-cycles of the multivibrator is determined by the time-setting circuits respectively R_1, C_1, and R_2, C_2:

$$T_1 = C_1 R_1 ln\,(U^1 / U^1_{1min}),\ T_2 = C_2 R_2 ln\,(U^1 / U^1_{1min}),$$

and the frequency of oscillations generated by $f = (T_1 + T_2)^{-1}$.

The capacitance of capacitors *C1*, *C2* defining the duration of the intervals T_1, T_2 is determined from the given ratios, respectively, for the selected resistance values of resistors *R1*, *R2*.

13.4.3. MV on the Schmitt trigger (TS)

Scheme MV on the Schmitt trigger is shown in Fig.13.12.

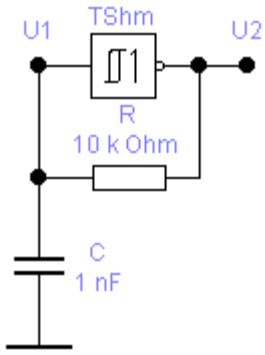


Fig. 13.12

If the multivibrator is to provide only a given frequency of generation *f* and the duty cycle is insignificant, it is advisable to use the scheme of the simplest multivibrator based on the Schmitt trigger.

The transfer characteristic of the Schmitt trigger has a pronounced hysteresis character. It distinguishes two threshold voltages U_{n1} and U_{n2} of switching the output voltage $U_2^1 \longrightarrow U_2^0$ and $U_2^0 \longrightarrow U_2^1$ respectively.

The simplest multivibrator is based on the inverting Schmitt trigger is the inclusion of an integrating *RC*-link between output and input.

At the moment of connection of the power supply U_{un} capacitor *C* is discharged, $U_1 = 0$, a high level is set at the inverting output of the trigger, which determines the charge of the capacitor through the resistor *R* with a constant time

$$\tau_1 = C(R+R^1_{вих}),$$

where $R^1_{вых}$ - the output resistance of the Schmitt trigger in the state "1" at the output.

In the new TS state, the input voltage drops exponentially as it approaches U_2^0. When U_1 compared to U_{n2}, the trigger switches to a new high output state, and a new charge cycle begins. Thus, the multivibrator excites itself, generates rectangular pulses, duration T1, and pauses T_2, which are determined by the ratios:

$$T_1 \approx \tau_1 \cdot \ln\left[\frac{U_2^1 - U_{n2}}{U_2^1 - U_{n1}}\right],$$

$$T_2 \approx \tau_2 \cdot \ln\left[\frac{U_2^0 - U_{n1}}{U_2^0 - U_{n2}}\right] = \tau_2 \cdot \ln\left[\frac{U_{n1}}{U_{n2}}\right].$$

These expressions allow us to calculate the frequency $f = \frac{1}{T} = \frac{1}{T_1 + T_2}$ of multivibrator generation and the duty cycle of output pulse:

$$\Theta_1 = (T_1+T_2)/T_1 = T/T_1\,, \quad \Theta_2 = (T_1+T_2)/T_2 = T/T_2.$$

The frequency stability of the multivibrator is low, since the difference in the transfer of voltages U_{n1} and U_{n2} is insignificant and the temperature drift of each of them significantly affects the duration of the time intervals T_1, T_2.

13.4.4 MV based on an operational amplifier

The scheme of MV based on the operational amplifier (OA) is shown in Fig.13.13.

Operational amplifiers are widely used in the construction of multivibrators because they have the following positive properties:

- high voltage gain ($K_U = 10^3 ... 10^5$) that guarantees self-excitation conditions;
- large drop in output voltage, the levels of which are close to the voltage of the power sources;
- large input and low output resistance;
- high rate of change of the output voltage S = V / s.

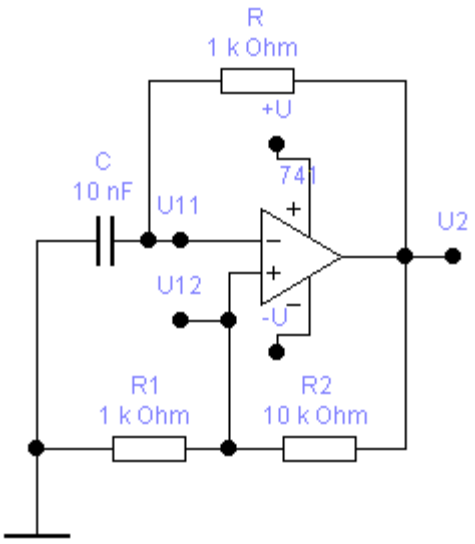


Fig.13.13

To provide a regenerative mode of switching, the OA is covered by positive feedback (Fig. 13.14), resulting in a transfer characteristic that acquires a hysteresis character similar to that of the Schmitt trigger.

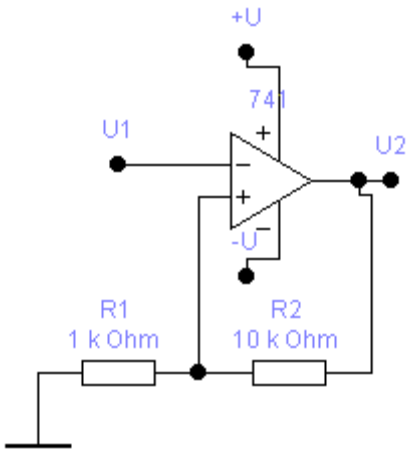


Fig. 13.14

The scheme in Fig.13.14 is a Schmitt trigger on the OA. The threshold voltages U_{n1}, U_{n2} of such a trigger are determined by the part of the output voltage supplied by the positive feedback circuit (*R1, R2*) to the non-inverting input.

Since the output voltage of the OA in the mode of the Schmitt trigger can accept only two static levels corresponding to the levels of positive U_{01} or negative U_{02} constraints , the threshold voltages are determined by the ratios:

$$U_{n1} = U_{o1} R_1/(R_1 + R_2) = U_{o1} ß \; ; \; U_{n2} = -U_{o2} R_1/(R_1 + R2) = -U_{o2} ß,$$

where $ß = R_1/(R_1 + R_2)$.

The multi-vibrator based on the Schmitt trigger on the OA can be obtained by introducing a connection between the output of the OA and its inverting input through an integrating *RC*-circuit. The principle of operation of such a multivibrator is to monitor the voltage delay at the inverting input U_{11} by the voltage at the non-inverting input U_{12}, which repeats virtually inertia with a coefficient of proportionality $ß < 1$ output voltage U_2. At the interval T_1 at the output of the OA, a high level was established, at the non-inverting input there is also a practically constant potential $U_{n1} = U_{o1} ß$, and at the inverting voltage the voltage exponentially approaches $U^+_{11} \rightarrow U_{o1}$ *as the charge of the capacitor C is constant*:

$$\tau_1 = C(R + R^+_{вих.}) \approx CR,$$

where $R^+_{вых}$ - the output resistance of the OA in the positive limit mode.

The charge of the capacitor C causes a decrease in the differential input voltage $U_d = U_{12}-U_{11}$ and when it reaches $U_d = U_{12} - U_{11} \approx 0$ OA goes into active mode. Under the influence of positive feedback, the Schmitt trigger switches to a low-output state. During the switching, the voltage on the capacitor C does not have time to change significantly, so the negative feedback (RC) on the switching processes has no effect. At the non-inverting input of OA the voltage $U_{p2} = -U_{o2}\,ß$ is set.

At interval $_{T2,}$ the voltage across capacitor C approaches with a constant time:

$$\tau_1 = C(R + R^{-}_{вих.}) \approx CR,$$

where $R^{-}_{вых}$ - the output resistance of the OA in the mode of negative limitation.

The interval T_2 ends at the moment of coincidence $U_d = U_{12} - U_{11} \approx 0$ and subsequent regenerative switching of the OA to the state of positive restriction. The duration of the intervals T_1, T_2 is determined by the exponential capacitor recharge functions in the voltage range between U_{n1} and U_{n2}:

$$T_1 = \tau_1 \ln [(U_{o1} - U_{n2})/(U_{o1} - U_{n1})],$$
$$T_2 = \tau_2 \ln [(-U_{o2} - U_{n1})/(-U_{o2} - U_{n2})].$$

Whereas $U_{n1} = U_{o1}\,ß$; $U_{n2} = = -U_{o2}\,ß$, the above relations can be represented in the form:

$$T_1 = T_2 = RC \ln [(1 + ß)/(1 – ß)] = RC \ln [(2R1 + R2)/R2],$$

i.e. the multivibrator generates rectangular pulses with an opacity of $\theta = 2$. An independent setting of the duration T_1, T_2 and the required velocity θ is realized when a nonlinear bipolar circuit replaces the resistor R.

13.4.5. MV on RS – trigger

The scheme of MV based on the RS-trigger is shown in Fig.13.15.

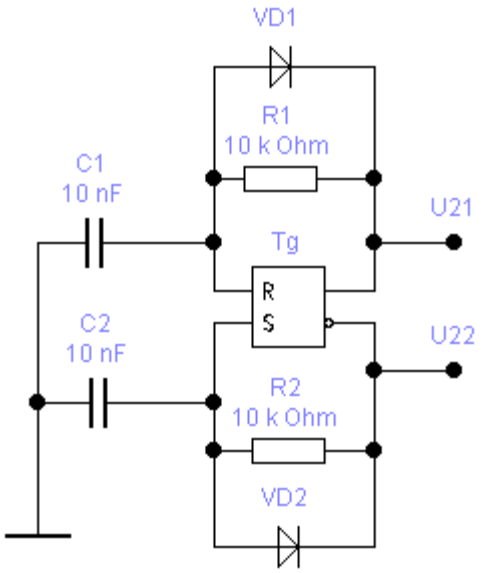


Fig.13.15.

To implement a multivibrator based on the *RS*-trigger, it is necessary to include two circuits defining the time parameters of the MV between the outputs and their respective inputs. Therefore, we get a self-oscillating multivibrator with independent control of half-time durations and time constants:

$$\tau_1 = C_1(R_1 + R^1_{вих}),\ \tau_2 = C_2(R_2 + R^1_{вих}),$$

where $R^1_{вых}$ is the output impedance of the *RS*-trigger in the state "1" at the output.

The duration of half-periods is determined by the ratios:

$$T_1 = C_1(R_1 + R^1_{вих})\ ln\ [(U^1_{21} - U^0_{21})/(U^1_{21} - U_{пор})],$$

$$T_2 = C_2(R_2 + R^1_{вих})\ ln\ [(U^1_{22} - U^0_{22})/(U^1_{22} - U_{пор})],$$

where $U_{пор}$ is the threshold switching voltage of the trigger.

Discharge of capacitors *C1, C2* flows rapidly through diodes *VD1, VD2* with constant time:

$$\tau_{p1} = C_1(r_{пр} + R^0_{вих}) \ll T_1\ ,\quad \tau_{p2} = C_2(r_{пр} + R^0) \ll T_2$$

and does not affect the frequency of generation:

$$f = (T_1 + T_2)^{-1.}$$

This multivibrator can be implemented on both TTL and CMDC IC. The relative disadvantage of such a MV is the temperature instability of the frequency (duration) of the pulses that are generated.

13.4.6. MV on two operational amplifiers

To increase frequency stability, it is possible to replace the relaxation processes occurring in exponential time linear circuits in linear circuits. Linear relaxation can be realized with a constant-level integrator. The scheme of such a multivibrator is a series connection in the closed circuit of the inverting integrator on the OA *DA2* and the non-inverting Schmidt trigger on the OA DA1 (Fig.13.16).

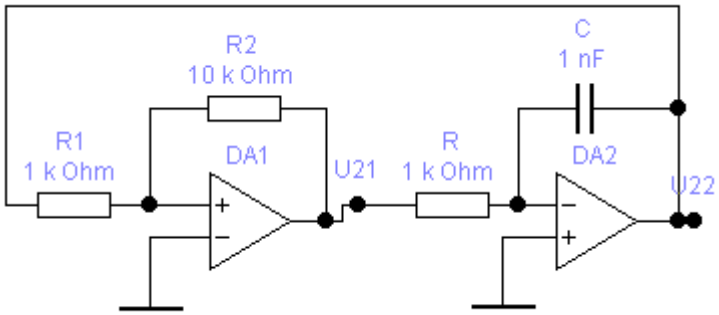


Fig.13.16

The transfer characteristic of a non-inverting Schmitt trigger is characterized by two threshold levels. The switching thresholds of the trigger U_{n1}, U_{n2} are determined by the resistance resistors *R1* and *R2* of the positive feedback at two possible voltage levels at the output of the Schmitt trigger:

$$U_{n1} = -U^{+}_{o} R_1/R_2, \quad U_{n2} = U^{-}_{o} R_1/R_2,$$

where U^{+}_{o}, $-U^{-}_{o}$ are the output voltage levels of the Schmitt trigger in states of positive and negative constraints, respectively, determined by the supply voltages of the operational amplifier.

The output voltages of the Schmitt trigger U^{+}_{o}, $-U^{-}_{o}$ are the input voltages of the integrator whose voltage at the output varies according to a linear law between the threshold levels U_{n1}, U_{n2}.

At the time interval T_1 the output voltage of the integrator decreases linearly from the initial value U_{n2}:

$$U_{21}(t) = U_{n2} - U^{+}_{o} t / (RC).$$

At the end of the interval T_1, the output of the integrator sets the voltage U_{n1} switching the output of the Schmitt trigger to the state $-U^{-}_{o}$. So

$$U_{21}(T_1) = U_{n2} - U^{+}_{o} T_1/ (RC) = U_{n1}.$$

From this relation we obtain an expression for the length of time interval T1:

$$T_1 = RC (U_{n2} + U_{n1}) / U^{+}_{o} = RC\, k (U^{+}_{o} + U^{-}_{o})/ U^{+}_{o},$$

where $k = R_1/R_2$.

Similarly, we obtain the expression for the time interval T_2:

$$T_2 = RC (U_{n2} + U_{n1}) / U^{-}_{o} = RC\, k (U^{+}_{o} + U^{-}_{o})/ U^{-}_{o}.$$

If the operating amplifier has symmetrical power, i.e. $U^{+}_{o} = |-U^{-}_{o}|$, duration T_1 and T_2 can be calculated by the expression:

$$T_1 = T_2 = 2kRC.$$

The output U_{21} of the multivibrator produces a series of rectangular pulses of the type "meander", and at the output U_{22} - pulses of triangular shape with frequency

$$f = (4kRC)^{-1}$$

and with the duty cycle θ = 2.

If it is necessary to obtain output pulses with arbitrary magnitude, the resistor *R* of the integrator must be replaced by a nonlinear bipolar.

The frequency stability of such a multivibrator is determined by the stability of the parameters of the components *R*, *R1*, *R2*, and *C*.

13.5. Generators of linear output voltage

Generators of linear output voltage (LOV) are electronic devices whose output voltage changes linearly for a specified time.

A number of parameters characterizes the linearly variable voltage U (t):

- the duration of the running stroke t_p, that is, the time during which a linearly output voltage is formed;
- the duration of the reverse $t_в$ (recovery time) is the time, during which the reverse transitions to the beginning of the linear portion of the output signal;
- the repetition period of the output signal $T = t_p + t_в$;
- amplitude *f* saw tooth pulses U_m;
- nonlinearity coefficient ε.

One of the most important parameters of the LOV is its coefficient of nonlinearity ε. To determine nonlinearity coefficient ε, we use the well-known assertion that a linear function is characterized by a constant derivative at all its points, so the deviation from the linear law can be estimated by the coefficient of nonlinearity. Nonlinearity is determined by the maximum deviation of the real waveform from the ideal linear shape. The coefficient of nonlinearity is found as the ratio of the difference of the maximum and minimum derivatives of the function on the working area of the signal to the maximum derivative:

$$\varepsilon\,(\%) = \frac{[\frac{dU(t)}{dt}]\max - [\frac{dU(t)}{dt}]\min}{[\frac{dU(t)}{dt}]\max} 100 \cdot$$

13.5.1. LOV generator on the dinistor (Shockley diode)

The scheme of the MV based on the dinistor (Shockley diode) and the operational amplifier is shown in Fig.13.16.

In the scheme of Fig.13.17, the resistance of the resistor R and the voltage of the power supply U_{cc} are chosen such that the load line intersects the voltage-current characteristic (VCC) of the dinistor with the parameters of switching up U_{max} and switching off U_{min} on the negative resistance section (to ensure the mode of generation).

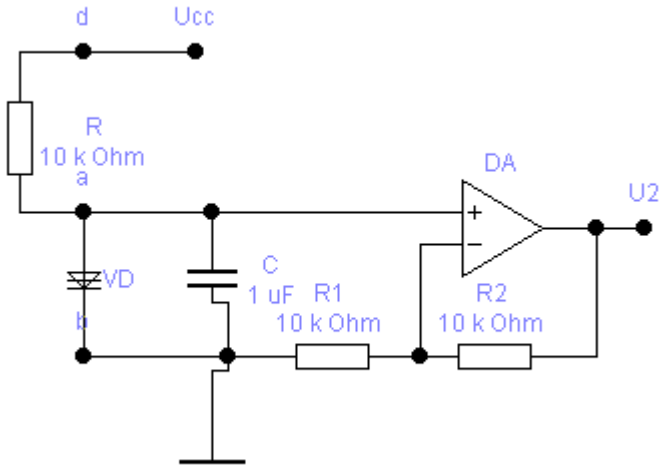


Fig.13.17

When the power is turned on through the resistor R, the charging of the capacitor C with a constant exponent $\tau_{зар} = CR$ starts $_{when}$ the capacitor is switched off. When U_c reaching U_{max}, the breakdown of the dinistor begins to switch on, its resistance is regenerative reduced to r_{np}. When dinistor is opened, the capacitor C is discharging through it, and at the moment when the voltage on it U_c reaches U_{min}, the dinistor shuts off and a new charge cycle of the capacitor C through the resistor R begins. The duration of the running stroke t_p or the exponential growth law is determined by the relation:

$$t_p = \tau_{зар} \ln [(U_{cc} - U_{min})/(U_{cc} - U_{max})] = RC \ln [(U_{cc} - U_{min})/(U_{cc} - U_{max})].$$

The duration of recovery, that is, the return tv also for the exponential law of reducing the voltage on the capacitor C with constant $\tau_{роз} = Cr_{np}$ is determined by the relation:

$$t_в = \tau_{роз} \ln (U_{max}/U_{min}) = Cr_{np} \ln (U_{max}/U_{min}) \ll t_p.$$

Thus, the frequency of generation of saw tooth output signals is:

$$f = (t_p + t_в)^{-1}.$$

The amplitude U_m of the output signals depends on the parameters of the components of the negative feedback and is determined by the ratio:

$$U_m = (U_{max} - U_{min})(1+R_2/R_1).$$

To ensure linearity of the signal work area, it is necessary to use the exponential initial section, that is, to select a dinistor so that the requirement is satisfied: $U_{max} \ll U_{cc}$. This condition is easily fulfilled if the *VD* dinistor is replaced by the scheme shown in Fig.13.18 by including it between points *a* and *б*. The maximum voltage on the capacitor *C* (instead of the parameter U_{max}) is determined by the control voltage U_{cm}.

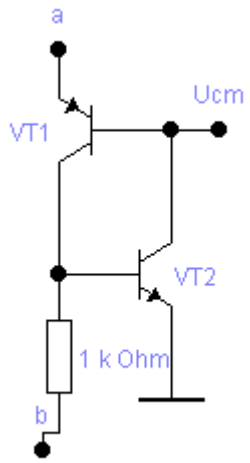


Fig.13,18

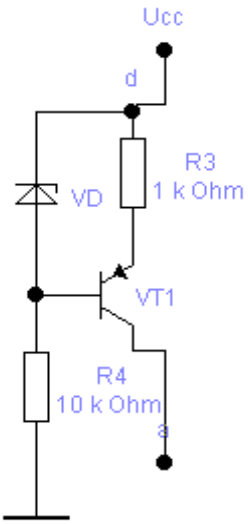


Fig.13.19

The nonlinearity of the signal work area can be significantly reduced if, if use instead of the resistor *R*, the generator constant current shown in Fig. 13.19, which is connected between points d and a. In this case, the capacitor *C* is charged by the generator constant current of the collector I_k of the transistor *VT1*, which is determined by the ratio:

$$I_k = (U_{st} - U_0)/R_3 = const,$$

where U_{st} - the stabilization voltage of the Zenner diode *VD*,
U_0 - voltage drop at the emitter junction of transistor *VT1*.

In this case, the voltage across the capacitor *C* increases according to a linear law:

$$U_c(t) = U_{\min} + \frac{I_k}{C}t$$

and the duration of the linear portion of the signal, when the signal increases from U_{min} to U_{max}, is:

$$t_p = (U_{max} - U_{min})C/I_k.$$

13.5.2. Shaper of LOV on an operational amplifier

The scheme of the shaper LOV based on the operational amplifier is shown in Fig.13.20.

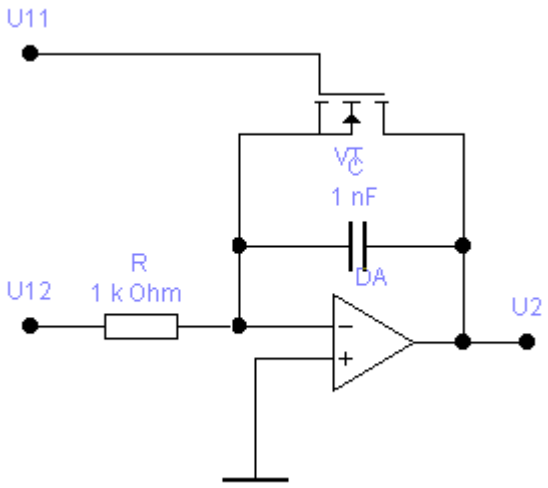


Fig.13.20

The shaper is based on an integrator on an operational amplifier covered by negative feedback due to the *RC* circuit. Transistor *VT* is used to set zero initial conditions. If the voltage at its gate $U_{11} > U_{nop}$, the channel is induced and has a low resistance R_i, shorting the capacitor C. This determines the initial conditions of integration:

$$U_{20} = - U_{12} R_i /R.$$

If the ratio $R_i \ll R$ is chosen correctly, we have $U_{20} \approx 0$, i.e. almost zero initial integration conditions when the capacitor *C* is practically discharged.

If a rectangular pulse of amplitude $U_{11} < U_{nop}$ is input to U_{11}, the *VT* transistor closes and capacitor *C* begins to charge by the currant:

$$I_C = I_R = U_{12}/ R.$$

The output of the integrator generates a voltage:

$$U_2(t) = U_{20} - \frac{1}{C} \int U12\, dt.$$

If U_{12} = const, then $I_C = I_R$ = const and the output signal over the duration t_p of the input pulse U_{11} is formed by a linear law:

$$U_2(t) = U_{20} - \frac{1}{C}\frac{U12}{R}t.$$

At the end of the input pulse t_p output voltage reaches the amplitude value:

$$U_{2m} = - U_{12\,tp}/(RC).$$

After the input pulse, the transistor opens and through it the capacitor C is discharged. Duration of recovery time

$$t_в \approx 3\,C\,R_i\,.$$

The considered scheme provides a high quality output signal with a low coefficient of nonlinearity and high load capacity.

14. Digital to analog and analog to digital converters

Digital to analog converters (DAC) are a class of devices that realize the conversion of code combinations (dimensionless quantities) into some physical value (most often, voltage) according to some conversion factor. DAC have a very wide range of applications in measurement, computing, biomedical engineering, transmission, storage and display information, in process control systems, etc. In the Ukrainian literature, DAC stands as ЦАП.

Schemes of use of digital-to-analog converters apply not only to the field of code-to-analog conversion. Using their properties, you can determine the composition of two or more signals; build function divisors, analog units controlled by microcontrollers, such as attenuators, integrators and more. An important area of DAC is also signal generators, including arbitrary waveforms.

The main function of the DAC is:

$$U(X) = K\times X_n,$$

where X is some digital code that, in the case of *n*-bit binary encoding, looks like:

$$\boldsymbol{X_n} = \sum_{i=0}^{n-1} x_i * 2^{\mathrm{i}},$$

where xi is the value of the i-th bit of the binary code: xi $\subset\{0,1\}$. The coefficient K determines the scale of conversion and has usually a dimension of voltage.

The conversion error reflects the difference between the nominal conversion function and the real one. This parameter can be specified both before the output and

before its input. If the conversion error is output, then it is expressed in units of output (voltage or current), if input, then in dimensionless portions of the unit of the converted code.

14.1. DAC based on analog adder

The scheme of DAC based on the analog adder is presented in Fig. 14.1. The principle of such a DAC is based on the addition of each bit current I_i, proportional to the weight of the bits number and which are controlled by the switchable logic variables xi of the converted code. The value of the bits current I_i is determined by the value of the reference voltage U_{on} and the resistance of the resistor of the i-th bit R_i:

$$I_i = U_{оп} / R_i .$$

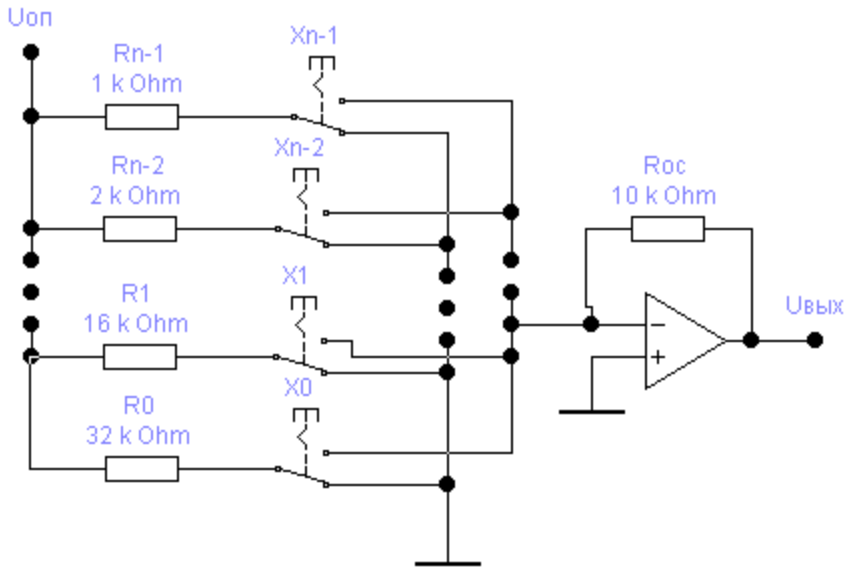


Fig. 14.1

The highest bit x_{n-1} of the converted code corresponds to the maximum bit current I_{n-1}, which is determined by the smallest resistance R_{n-1}. The current of the second bit I_{n-2} is twice less, that is, the resistance R_{n-2} accordingly twice. The minimum input current gives a lower bit x_0 and corresponds to the maximum resistance R_0.

That is, the resistance in the circuit of the *i-th* binary code should be equal to:

$$R_i = R_0/2^i.$$

Connecting of the bit current I_i to the input of the operational amplifier or switching it to "ground" is carried out by the electronic switch, shown in Fig. 14.2.

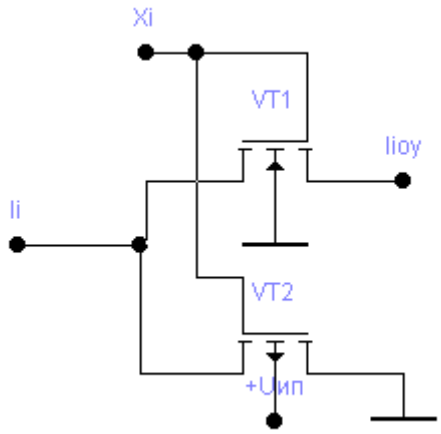


Fig. 14.2

If $x_i = 0$, transistor *VT2* is open and *VT1* is closed and current I_i is disconnected from the input of the operational amplifier. At $x_i = 1$, the transistor *VT1* is opened and the current of the current I_i is fed to the input of the operational amplifier together with other bit currents. Thus, the total current supplied to the operational amplifier is determined by the expression:

$$I(U_{on}, R_i, x_i) = \sum_{i=0}^{n-1} x_i I_i = U_{on} \sum_{i=0}^{n-1} x_i / R_i = U_{on}/R_0 \sum_{i=0}^{n-1} x_i 2^i = U_{on} \boldsymbol{X_n} / R_0,$$

where $\boldsymbol{X_n}$ is the input digital code.

Almost all of these currents flow through the resistor R_{oc} of the feedback circuit in the operational amplifier (OA), since the OA's own input current is disappearing small. Then the output voltage of such DAC is equal to the voltage drop across the resistor in the feedback circuit R_{oc} (taking into account the sign):

$$U_{вых} = - R_{oc} \times I(U_{оп}, R_i, x_i) = - R_{oc} U_{оп} \boldsymbol{X_n} / R_0.$$

At high bit DAC, current-setting resistors must be determined with high accuracy. The most stringent precision requirements are imposed on the higher-order resistors, since the current variance in them must not exceed the current of the lower-bit current. Therefore, the variation of the resistance denominations in the *i-th* bit R_i must be no more than $\delta R_i / R_i (\%) = 100 / 2^{i+1}$.

From this condition it follows that the variation of the resistor resistances, for example, in the fourth digit should not exceed 3%, and in the 10-th digit - 0.05%.

The above DAC scheme is simple, cheap, the ability to convert binary-decimal codes without first recoding into binary code. Its performance is uniquely determined

by the frequency properties of the OA and the performance of the transistors of the electronic switch on transistors *VT1*, *VT2*.

The scheme under consideration has a number of disadvantages. The main one is the need for a large number of precision resistor types. In addition, the resistance of the higher-order resistors in the multi-bit DAC can be comparable to the resistance of the locked key, which causes an additional conversion error. These disadvantages limit the allowable bit of conversion codes. As a rule, for such schemes have no more $n \leq 6$.

Figure 14.3 shows the DAC graphic designation in a Workbench environment with an output voltage proportional to the digital code.

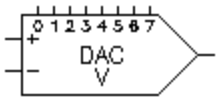


Fig. 14.3

14.2. DAC based on *R - 2R* series of resistors

To eliminate the main disadvantage of circuits based on the analog adder, a DAC scheme based on the *R-2R* resistor line, shown in Fig.14.4, has been developed and widely used. Resistors *2R* of such line through electronic switches on transistors *VT1*, *VT2* (Fig. 14.5) are connected by a logical signal x_i either to ground through transistor *VT1*, or to a potentially grounded input of an operational amplifier. Therefore, the current of the lowest bit x_0 is determined by the resistance of the resistor *2R* and the node voltage, which is the result of the separation of the reference voltage U_{on} for the discharge x_1 between the resistor *R* and the parallel connection of the two *2R* resistors, that is, half the voltage.

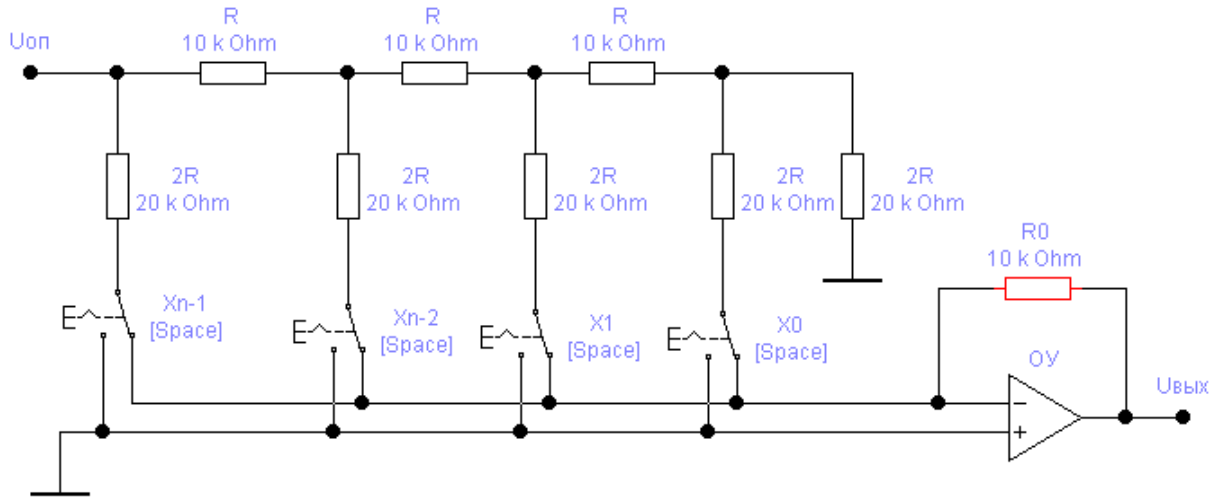


Fig. 14.4

For the i-th order, the node voltage is:

$$U_i = U_{on} / 2^{n-1-i}.$$

Then the current of the i-th order I_i is determined by the expression:

$$I_i = U_i / 2R = U_{on} / (2R * 2^{n-1-i}) = U_{on}\, 2^i / (R\, 2^n).$$

The input of the OA, taking into account the action of logical variables x_i receives a current signal equal to:

$$I_{oy} = \sum_{i=0}^{n-1} x_i I_i \ .$$

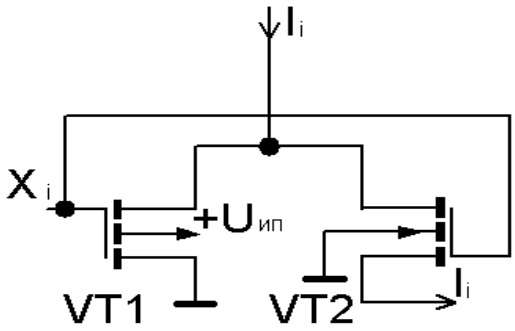


Fig. 14.5

This current, flowing mainly through a resistor in the negative feedback circuit R_0, generates an output voltage:

$$U_{вых} = - I_{on} R_0 = - R_0 \sum_{i=0}^{n-1} x_i I_i = - R_0 U_{on} / (R\, 2^n) \sum_{i=0}^{n-1} x_i 2^i = - R_0 U_{on} X_n / (R\, 2^n) = \Delta U X_n,$$

where the value of $\Delta U = R_0\ U_{on}\ /\ (R\ 2^n)$ is a discrete amount of voltage corresponding to the minimum increment of the output voltage, i.e.. the contribution of the smallest bit to the output signal.

The main advantage of the DAC discussed in this section is the minimum number of precision resistor types - only 2 (*R* and *2R*). Main disadvantage is due to the non-ideality of the electronic switches, the resistance of which is added with a resistance of *2R* and introduces a corresponding statistical error, and in this DAC there is. However, the number of such DACs is greater (n = 10 ... 12) and their application is wider.

14.3. DAC on current switches

The design of the DAC on diode current switches is to eliminate the influence of the resistance of non-ideal electronic keys on the value of the controlled variable bits of current. For this purpose it is necessary to ensure the formation of each bit currents from sources with the maximum possible internal resistance (preferably, from an ideal current source), the value of which could not be affected by the internal resistance of the electronic key. As such a current source with very high internal impedance can be used bipolar transistor included in the scheme with a common base.

In Fig.14.6 is shown DAC circuit based on the *R-2R* resistive matrix, bipolar transistors VT_0,… VT_{n-1} included in the common-base circuit, and switches for the bit currents of diodes VD1, VD2.

Currents of each bit are formed by the resistor matrix *R-2R*. The potentials of the transistor bases are the same and offset by the $R_б$ – VD_0 circuit so, that the transistor emitter potentials are approximately zero. Then the currents of the emitters of the transistors are determined by the node voltages formed by the resistor matrix *R-2R*.

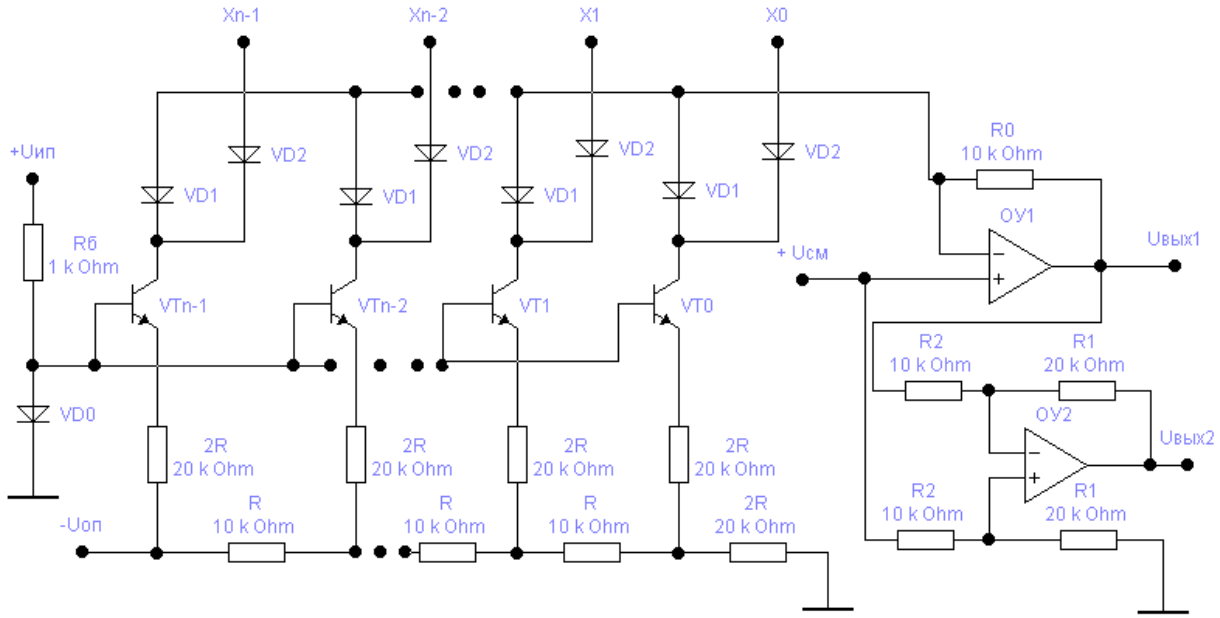


Fig. 14.6

For the transistor *VTn-1*, this voltage is Un-1 = - U_{on}, for the *VTn-2* transistor it is twice less than the absolute value: U_{n-2} = - U_{on} / *2* and further, at the transition from node to node, the voltage is halved. For the i-th bit, the node voltage is:

$$U_i = – U_{on}/2^{n-1-i}.$$

Then the emitter current of the *i*-th transistor is determined by the expression:

$$I_{эi} = U_i/2R = U_{on}/(2^{n-1-i}*2R) = U_{on}/(R\,2^{n-i}).$$

Accordingly, the current of the collector of the *i*-th transistor is constant and is equal to:

$$I_i = \alpha I_{эi} \approx U_{on}/(R\,2^{n-i}),$$

where $\alpha \approx 1$ is the current transfer ratio of the transistor in the scheme with a common base.

The collector currents of the each bit transistors flow either through the diode *VD1* if the logic variable of the discharge code is low ($x_i = 0$) and the diode *VD2* is closed or through the diode *VD2* if the logical variable discharge is high ($x_i = 1$). That is, if the diode *VD1* is closed and *VD2* is open, and if the diode *VD1* is open and *VD2* is closed.

Currents of *VD1* diodes are added and form the total current:

$$I_\Sigma = \sum_{i=0}^{n-1} I_i = \sum_{i=0}^{n-1} \frac{U_{on} x_i}{2^{n-i} R} = \frac{U_{on}}{2^n R} \sum_{i=1}^{n-1} x_i 2^i \quad ,$$

which flows mainly through resistor R0 in the negative feedback loop of the operational amplifier OA. At its output, taking into account the bias voltage U_{cm} formed voltage:

$$U_{вых1} = U_{см} - I_\Sigma R_0 = U_{см} - \frac{R_0}{R}\frac{U_{on}}{2^n}\sum_{i=0}^{n-1} x_i 2^i = U_{см} - \frac{R_0}{R}\frac{U_{on}}{2^n} X_n,$$

where X_n - the input digital code.

The bias voltage U_{cm} is required to ensure the normal active mode of transistors $VT_0 \ldots VT_{n-1}$. To neutralize the voltage U_{cm} and simultaneously scaling the output voltage of the DAC uses a subtraction scheme for OA2. At its output voltage is equal to:

$$U_{вых2} = \frac{R_1 R_0}{R_2 R}\frac{U_{on}}{2^n} X_n \ .$$

The main advantage of this DAC is that its output voltage is almost independent of the resistance of the electronic keys (in this case, diodes *VD1* and *VD2*). This makes it possible to increase the maximum digit of conversion codes: $n \le 14$.

The disadvantage of this scheme is the operation of bipolar transistors in active mode, which increases the power, dissipated on the collectors of the transistors, and

have to solve the problem of heat removal. Highest power is dissipated on the *VTn-1* transistor.

14.4. ADC of deployment compensation

The principle of operation of analog-to-digital converters (ADC) is to measure the level of the input signal and output the result in digital form. As a result of the ADC, discrete samples of continuous analog signal are converted to the corresponding digital codes.

In order for the ADC to function properly, the input signal must not change during the conversion time, which is usually accompanied by a sampling-storage circuit that captures the instantaneous signal level and stores it throughout the conversion time. In Fig. 14.7 shows ADC of deployment compensation, that converts an analog signal U_a into an n-bit binary code X_n.

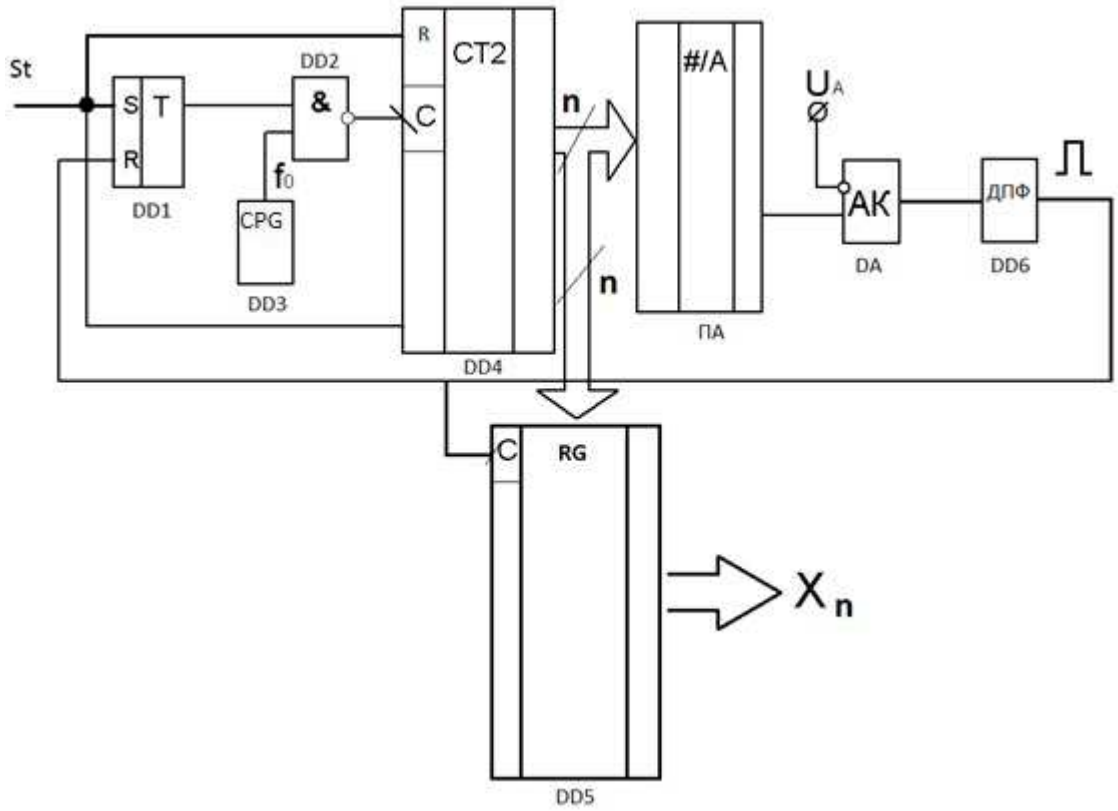


Fig. 14.7

This converter is a typical example of sequential one-way ADCs containing an RS-trigger, a clock pulse generator CPG, a n-bit binary counter CT, an analog comparator AK, a digital-to-analog converter ПА , and a n-bit register RG controlled by a signal output from a positive output front of the ДПФ. At the output of the register, RG generates the output code X_n. One input of the AK comparator receives an analog input signal U_A and the other inputs connected with a DAC ПА output.

The operation of the converter begins with the arrival of the startup pulse *St*, which sets in a state "1" RS-trigger, the output of which opens the *DD2* valve and pulses from the clock generator CPG with frequency f_0 are fed to the input of the binary counter CT2, which sums the number of input pulses. The output code of the counter is fed to the DAC, which converts it into voltage. The equilibration process lasts until the DAC output voltage equals or exceeds the input voltage U_A. At the time of comparison or exceeding the output voltage of the DAC with the analog voltage U_A, the analog comparator AK is triggered.

Switching the output of the comparator from "1" to "0" indicates the completion of the conversion process. The output code X_n is proportional to the input voltage at the end of the conversion.

The conversion time of this type of ADC is variable and depends on the input voltage. Its maximum value $t_{np.max}$ responds to the maximum input voltage and for the n-bit binary counter and clock frequency f_0 is equal to:

$$t_{пр.макс} = (2^n\text{-}1)/ f_0.$$

For example, at n = 10 and f_0 = 1MHz, $t_{пр.макс}$ = 1024 μs, providing a maximum sample rate of the order of 1 kHz.

When operating without a sampling-storage device, the aperture time coincides with the conversion time. As a result, the result of the conversion is extremely dependent on the ripple of the input voltage. In the presence of high-frequency ripples, the average value of the source code nonlinearly depends on the average value of the input voltage. This means that the ADCs of this type without the sampling-storage device are suitable for operation with constant or slowly varying voltages, which during the transformation change no more than the value of the conversion quantum.

Thus, the ADC of the deploying compensation is the low conversion rate, which reaches several kHz:

$$f_{изм.макс} \le 1/ t_{пр.макс} = f_0 / (2^n\text{-}1).$$

The advantage of ADC of this class is the comparative ease of construction, due to the consistent nature of the conversion process, and the disadvantage - low speed.

14.5. ADC following compensation

In Fig. 14.8 shows the scheme of the ADC following compensation, the main functional elements of which are a reversible binary counter CT2, digital-to-analog

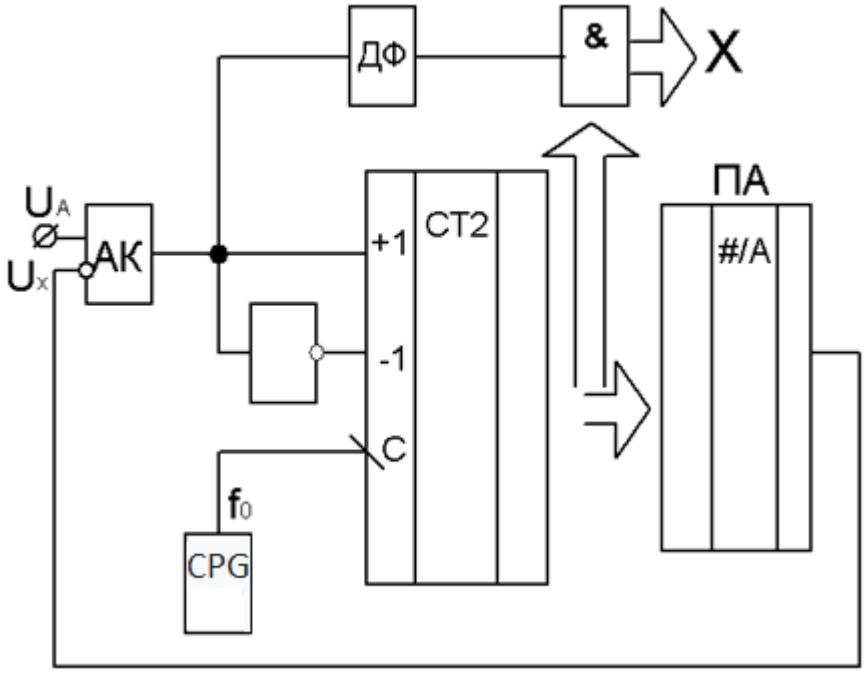
converter ПА , clock pulse generator CPG, analog comparator AK, detector positive and negative fronts ДФ and n-bit commutator of code X_n.

The principle of the ADC following compensation is based on the use of a reversible counter whose source code is converted by a digital-to-analog converter into a sampled voltage $U_Ц$. The voltage of the $U_Ц$ is compared with the input signal U_A of an analog comparator, which generates a signal U_k of the control of the direction of the counter account. Thus, a numeric code X_n is formed in the counter, which corresponds to the instantaneous value of the analog value U_A:

$$U_A = X_n \Delta U + \delta U,$$

where $\Delta U = U_{оп} / 2^n$,

δU - conversion error; moreover, $\Delta U \leq | \delta U |$.



In Fig. 14.8 shows a block diagram of the ADC following compensation.

Fig. 14.8

Clock pulses with a frequency f_0 are fed to the input of the counter CT2, the output code of which is converted into analog form and how the voltage Ux is supplied to the input of the comparator AK and compared with the converted analog voltage U_A. For example, if $U_x < U_a$, voltage of high level from comparator controlled the counter CT2 and it works in the sum mode. In time the value of voltage U_x steppedly increased and at $U_x > U_a$, the comparator switches the controlled input of the counter CT2 and turned it to the subtraction mode. When the detector has a DF

front, it forms an impulse, which means that the value of the digital code X_n corresponds at this moment to value U_a. From this moment the value of voltage U_x steppedly decreased to quiet feast leave $U_x > U_a$. At the moment of equals or $U_x < U_a$ the comparator will switch over and put the counter in the sum mode. When the detector is used, the front of the ДФ is redefined as a pulse of a specific value of the digital code X_n. In this way, the value of the output voltage U_x follows to changes of input voltage U_a.

For normal work of such an ADC, it is necessary to ensure that speed of change voltage of the analog signal U_a was smaller and then the speed of the speed of the output signals U_x of DAC. That means, that must be used condition:

$$dU_a/dt < \Delta U f_0 = U_{on} f_0/2^n ,$$

where ΔU is the quantum of the increase in the eddy spacing of the DAC, U_{on} is the bearing voltage of the DAC.

The smaller the speed of the input of the analogue signal dU_a / dt is, the higher is the frequency of the output code X_n. At U_a = const, the frequency of output code X_n is expensive f_0.

The advantage of such ADC is simplicity of structure, and disadvantage is asynchronism of the type of output code X_n.

14.6. Successive approximation ADC

A successive approximation converter ADC is the most widespread variant of successive ADC.

Work of this class of converters principle of dichotomy is the basis of, i.e. successive comparing of measured to 1/2, 1/4, 1/8 et cetera from her maximal possible value. It allows for *n*- bit of ADC to execute all process of transformation after *n* of successive steps (iterations) instead of 2^n times at the use of successive account and to score a substantial advantage in a fast acting. For example, already at $n = 10$ this winning arrives at 100 times and allows to get by means of such ADC to 10^5 ... 10^6 converting in a second. In the same time static error of this type of converters, that is determined mainly DAC, that is used, can be very small, that allows realizing a discriminability to 14 binary digits at frequency of selections of to 200 kHz.

Let us consider principles of construction and work of successive approximation ADC on the example of the structure brought around to Fig.14.9, that consists of next basic knots: clock pulse generator CPG, RS- trigger, register of successive approximation of РПП, digit-to-analog converter DAC, analog

comparator of АК, detector of positive fronts of ДПФ and n- bit register RG for storage and delivery of current values of digital code of X_n.

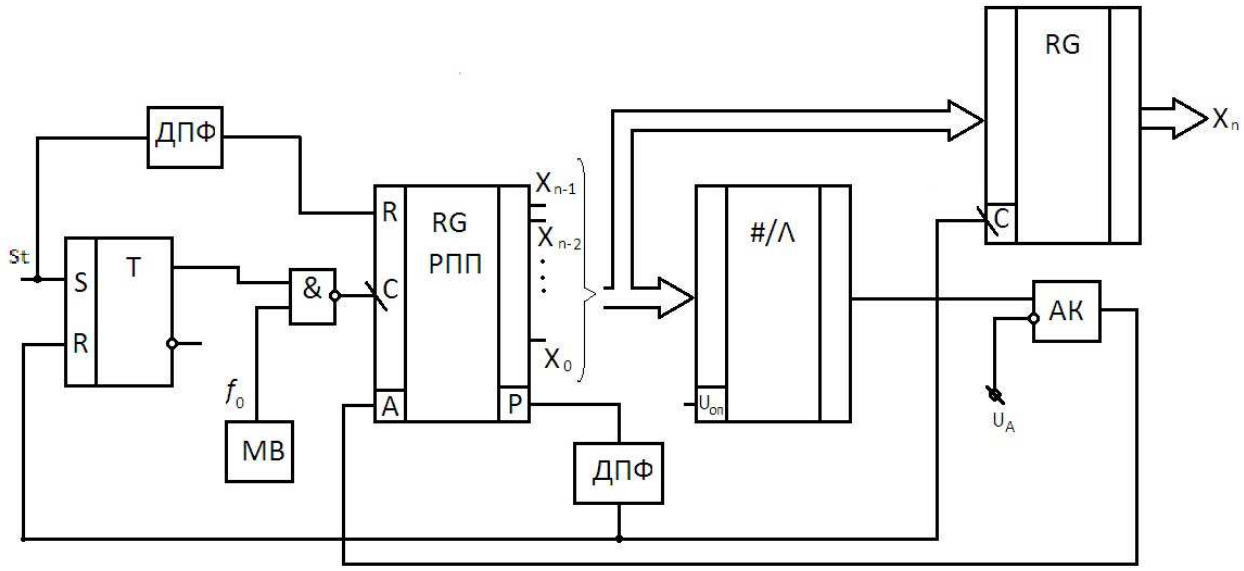


Fig. 14.9

The starting entrance impulse of St sets RS-trigger in the state "1" and n- bit register of successive approximation of РПП in the initial state, when in n-digit is brought "1", and in other digits - "0". Content of РПП will grow into an exit DAC. Output of DAC in analog form of $U_ц$ and compared on the analog comparator of АК with the current value of analog signal of U_a. If $U_ц < U_a$, the state of n- digit is fixed at the level of "1", and in case of $U_x > U_a$ the state of n- digit is fixed at the level of "0".

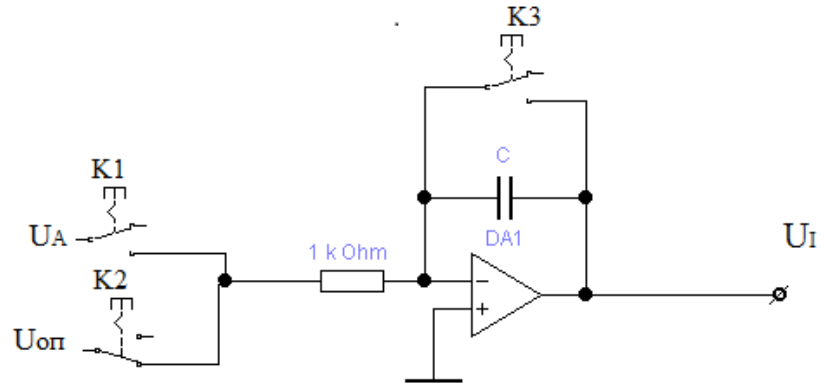
Next impulse brought "1" in the (n - 1)-th digit of РПП and like on the state the initial signal of analog comparator of АК the value of (n – 1)-th digit of source code is determined. At *n* times will be certain all *n* digits of code of X_n. Through *n* times on the exit of РПП the signal of overfilling of P is formed, that transforms the detector of positive fronts of ДПФ in the impulse of reset of RS- trigger in the state "0". The same impulse provides the transfer of content of register РПН as n- bit code of X_n in the register of RG, that corresponds to the current value of analog signal of U_a.

This class of АЦП occupies intermediate position after a fast acting, cost and discriminability between consistently parallel and integrating ADC and finds wide application in control system, control and digital treatment of signals.

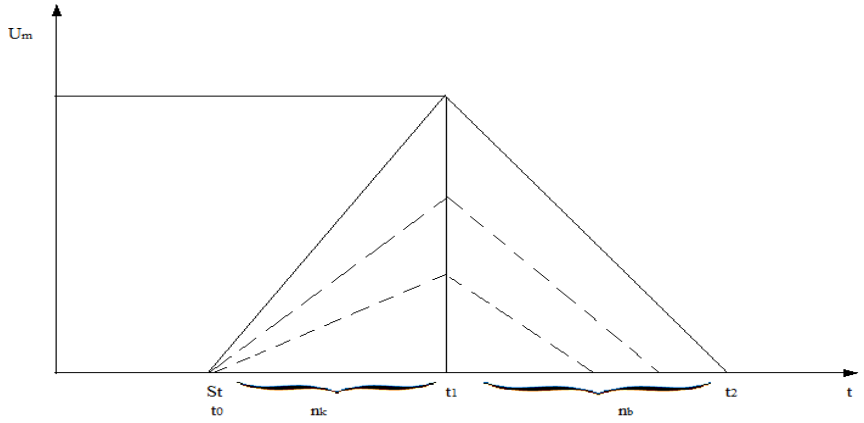
14.7. ADC of double integration

In fig. 14.10 are brought the principle over of transformation (б), analog integrator on an operating amplifier (а) and example of realization of ADC of double integration (в). Such ADC can be in one of the 3th states: accumulation, measuring, storage. For fixing of 3 states the used 2 RS-triggers (*Q1*, *Q2*). Output signals of

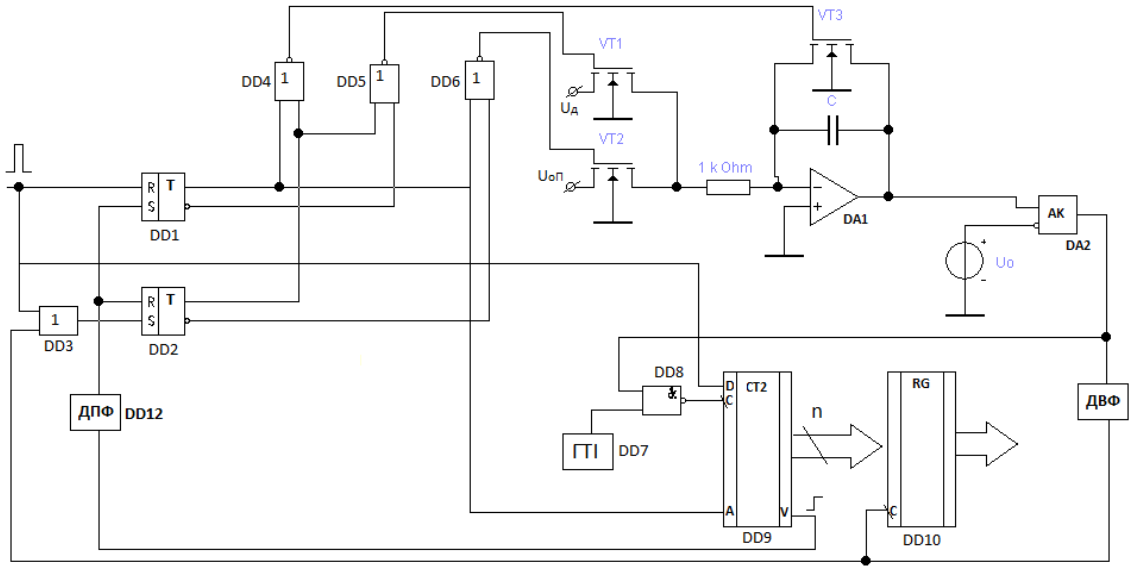
triggers used for a control by the keys of *K1 K2*, *K3* by signals accordingly *V1*, *V2*, and *V3*. In a table 14.7 the brought states over of triggers in accordance with time intervals and signals of control of the keys on the transistors *VT1*, *VT2*, and *VT3*.



а.



б.



в.

Fig. 14.10. ADC of double integration: а-conceptual chart; б- time diagram of transformation; в- fundamental circuit

Table 14.7

State	Time interval	Q_1	Q_2	V_1	V_2	V_3	Function V
Storage	$t < t_0; t > t_2$	0	0	0	0	1	$V_3 = \overline{Q_1} \cdot \overline{Q_2} = \overline{Q_1 + Q_2}$
Accumulation	$t_0 \le t \le t_1$	1	0	1	0	0	$V_1 = Q_1 \cdot \overline{Q_2} = \overline{Q_1 + Q_2}$
Measuring	$t_1 \le t \le t_2$	0	1	0	1	0	$V_2 = \overline{Q_1} \cdot Q_2 = \overline{Q_1 + Q_2}$

Work of ADC begun with the serve of starting impulse of St, that sets RS-trigger of *DD1* in the state of *Q1=1*, and RS-trigger of *DD2* confirms the previous state of *Q2= 0*. The same signal to the counter of *DD9* (entrance of D) is add the constant of $n_н$, that determines the fixed amount of times of accumulation of $n_н$. In accordance with the table of the states by the logical elements of NOR *DD4*, *DD5*, *DD6* is formed signals of *V1=1*, *V2=V3=0*, the key of *K1* on the transistor of *VT1* is switched on, and keys of *K2*, *K3* on transistors accordingly *VT2*, *VT3* states switched off. Through *VT1* the input analog signal of $\boldsymbol{U}_A$ (for shown example $\boldsymbol{U}_A < 0$) acts on the entrance of integrator of *DA1*. Increase of initial tension of integrator of *UI* > 0 stipulates establishment on the exit of analog comparator of *DA2* of high level of *U1k*, that provides the element of *DD8* serve of time impulses on the exit of *C* of meter of *DD9*. The mode of operations of the reversible counter is determined by the state of input A: at *A= 1* counter functions in the mode of subtraction, and at A = 0 - in the mode of add. After of $n_н$ times the state of counter changes from $n_н$ to 0, when on the exit of V of counter a high level (*V*=1) that grows the detector of positive fronts ДПФ of *DD12* into a short positive impulse is formed. Impulse from ДПФ (*DD12*) resets RS-trigger of *DD1* (*Q1=0*) and sets in the state of *Q2 =1* RS- trigger of *DD2*, that answers passing of ACD to the state of measuring. Thus signal of *V1*=0 switch off the key of *K1* on the transistor of *VT1*, and signal of *V2=1* switch on the key of *K2* on the transistor of *VT2*. On the input of integrator the fixed supporting voltage of $\boldsymbol{U}_{on}$ (in the set example of $U_{on} > 0$) is given on the output of integrator of voltage of $\boldsymbol{U}_I$ diminishes on a linear law. Thus on an entrance *A* of counter *DD9* operates the low level of *A=Q1=* 0, i.e. a counter functions in the mode of add. When the output level of integrator reaches level $\boldsymbol{U}_I \le 0$ (moment of time of t_2), the output signal of comparator is transfer in the state of $\boldsymbol{U}_K$ = 0, that blocks the receipt of impulses on the input of counter of *DD9*. Thus, in a counter the number of $\boldsymbol{X}_n$ is kept, that is the digital equivalent of analog quantity of U_A. The detector of negative fronts (ДВФ) of *DD11* forms a short positive impulse that reset RS- trigger of *DD3* in the state of *Q2=0* and ADC transfer in the mode storage to the next starting impulse of

St. Impulse from ДВФ is given on the input *C* of parallel register of *DD10*, in that the certain code of $\boldsymbol{X}_n$, which is proportional to the input voltage of U_A:

$$X_n = - U_A n_н / U_{оп}.$$

Time of transformation of ADC of this type is to the variables and depends on input voltage of $\boldsymbol{U}_A$. The maximal value of $t_{пр.макс}$ answers maximal input signal U_A and for n-bit binary counter and frequency of impulses of f_0 is:

$$t_{пр.макс} = (2^n + n_н)/f_0,$$

where $n_н$ - an amount of time interval of accumulation.

Basic advantages of the considered type of ADC are:

- it is independence of result of transformation from stability of parameters of integrator, that allows to realize ADC with the bit of output code of $n \leq 12$, without using of high-fidelity and high-stable components;

- the error of conversion does not depend on stability of parameters of components of integrator of *R, C* (range of parameters and their changing in time as a result of aging, change of temperature and others like that);

- the error of conversion does not depend on stability of frequency of f_0 of time generator, if frequency unimportant changes in continue to the interval of $t_0 \ldots t_2$. The error of the conversion depends only on stability of supporting voltage $U_{оп}$.

14.8. ADC of parallel transformation

The circuit of ADC of parallel conversion is shown in fig.14.11.

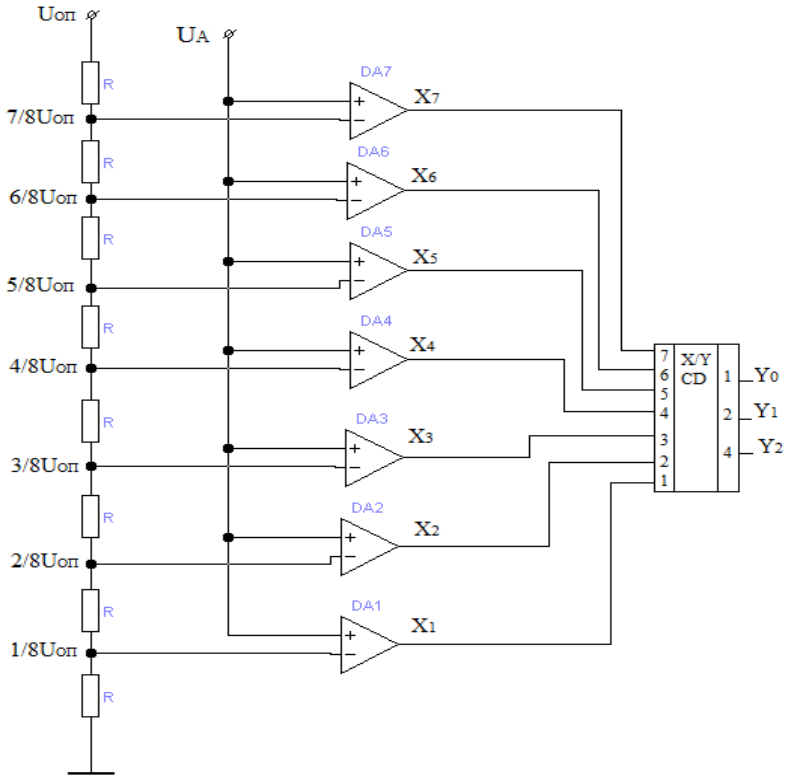


Fig. 14.11

In parallel ADC principle of direct comparison of analog quantity of $\boldsymbol{U_A}$ is used with the discrete values of supporting voltage of U_{on}.

In Table 14.8 is shown a comparison of analog voltage U_A with the discrete levels of supporting voltage of U_{on}, divided in this case into 8 ranges. Physical realization of discrete levels of the voltage with resistance divider is provided.

Comparing of input voltage U_A to the discrete levels is executed by the comparators of *DA1 - DA7*. If $U_A > U_{on} \times i / 8$, on the output of comparator is set X_i =1. Thus, on outputs of comparators appears a code (code of Johnson) that can be recorded in the binary code of $Y_2\ Y_1\ Y_0$ with the help of transformer of codes (X/Y) or with priority encoder (CD) (for to the most significant digits).

Table 14.8

Порівн. U_A з $U_{ОП}$	X_7	X_6	X_5	X_4	X_3	X_2	X_1	Y_2	Y_1	Y_0
$0 U_A < 1/8\ U_{ОП}$	0	0	0	0	0	0	0	0	0	0
$1/8\ U_{ОП} \le U_A < 2/8\ U_{ОП}$	0	0	0	0	0	0	1	0	0	1
$2/8\ U_{ОП} \le U_A < 3/8\ U_{ОП}$	0	0	0	0	0	1	1	0	1	0
$3/8\ U_{ОП} \le U_A < 4/8\ U_{ОП}$	0	0	0	0	1	1	1	0	1	1
$4/8\ U_{ОП} \le U_A < 5/8\ U_{ОП}$	0	0	0	1	1	1	1	1	0	0
$5/8\ U_{ОП} \le U_A < 6/8\ U_{ОП}$	0	0	1	1	1	1	1	1	0	1

6/8 $U_{ОП} \le U_A < 7/8\ U_{ОП}$	0	1	1	1	1	1	1	1	1	0
7/8 $U_{ОП} \le U_A$	1	1	1	1	1	1	1	1	1	1

The considered type ADC does not need synchronization of the process conversion. Forming of the output code of X_n will be realized with only time delay of passing of signal through a comparator and transcoder that provides the maximal fast-acting of ACD. It is necessary to mark that complication of circuit is doubled at the increase of bit of source code of n on $n+1$. For example, for n=8 it is necessary 255 comparators and corresponding encoder on 255 entrances. Therefore for realization of multibit parallel ADC use parallel-sequence ADC, that yet name conveyer.

14.9. Conveyer ADC

Principle of construction of conveyer ADC is based on determination of difference between input signal of U_A and the nearest the discrete level of U_{oni}, strengthening of the got difference to the range of U_A, following discretization of the distinguished and increase difference in the digital code of the least significant bits, selection to the difference, strengthening and further transformation. Example of such to the "conveyer" is made an in Fig.14.12.

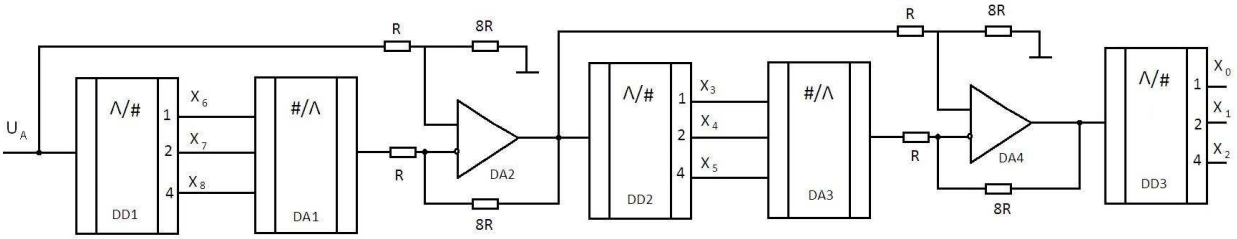


Fig. 14.12

On the first stage of transformation parallel ADC *DD1* converts input analog voltage of U_A into a 3-bit code ($x_8\ x_7\ x_6$) with the error of discretization $\Delta U1 < U_{ОП}/8$. Code of $x_8\ x_7\ x_6$ with a help a DAC *DA2* transfers into the analog quantity of $U_{Ц1}$. With the help of circuit of subtraction on the operating amplifier of *DA1* the error of discretization $\Delta U1 = U_A - U_{Ц1}$ is calculated, that simultaneously increases in 8 times, that means the down-scaling of error to the range of supporting tension of $U_{ОП}$:

$$U_{A2} = 8(U_A - U_{Ц1}).$$

On the second stage voltage of U_{A2} with the help of ADC *DD3* transfers into the code of the least significant bits of $x_5\ x_4\ x_3$, which DAC *DD4* converts into discrete voltage of $U_{Ц2}$. The circuit of subtraction – amplifying on *DA2* forms the analog signal of U_{A3}, which ADC *DD5* converts into the 3-bit code of $x_2\ x_1\ x_0$. The 9-bit code of $x_8x_7\ldots x_0$ thus formed that is the digital analogue of input level of U_A.

Note that all operation of transformation does not need synchronization of components of conveyer structure. The latest forming the least significant bits of $x_2\ x_1\ x_0$ with the delay time in the stages of the described structure. Therefore such a ADC is classified as parallel-consequent. They provide minimum time of t_n transformation of $U_A \rightarrow X_n$, i.e. maximal quantum frequency of analog signals:

$$f_{\text{п}\,max} \leq 1/t_{\text{п}}.$$